Appendix A
List of Memory Maps

Table A-1. SIM Registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x000	Reset status register (RSR) [p. 6-5]	System protection control register (SYPCR) [p. 6-8]	Software watchdog interrupt vector register (SWIVR) [p. 6-9]	Software watchdog service register (SWSR) [p. 6-9]
0x004	Pin assignment register (PAR) [p. 6-10]		Interrupt port assignment register (IRQPAR) [p. 9-7]	Reserved
0x008	PLL control (PLLCR) [p. 7-3]	Reserved		
0x00C	Default bus master park register (MPARK) [p. 6-11]	Reserved		
0x010–0x03C	Reserved			

Table A-2. Interrupt Controller Registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
Interrupt Registers [p. 9-3]				
0x040	Interrupt pending register (IPR) [p. 9-6]			
0x044	Interrupt mask register (IMR) [p. 9-6]			
0x048	Reserved			Autovector register (AVR) [p. 9-5]
Interrupt Control Registers (ICRs) [p. 9-3]				
0x04C	Software watchdog timer (ICR0) [p. 6-6]	Timer0 (ICR1) [p. 9-2]	Timer1 (ICR2) [p. 9-3]	I^2C (ICR3) [p. 9-3]
0x050	UART0 (ICR4) [p. 9-3]	UART1 (ICR5) [p. 9-3]	DMA0 (ICR6) [p. 9-3]	DMA1 (ICR7) [p. 9-3]
0x054	DMA2 (ICR8) [p. 9-3]	DMA3 (ICR9) [p. 9-3]	Reserved	

Table A-3. Chip-Select Registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x080	Chip-select address register—bank 0 (CSAR0) [p. 10-6]		Reserved[1]	
0x084	Chip-select mask register—bank 0 (CSMR0) [p. 10-6]			
0x088	Reserved[1]		Chip-select control register—bank 0 (CSCR0) [p. 10-8]	
0x08C	Chip-select address register—bank 1 (CSAR1) [p. 10-6]		Reserved[1]	
0x090	Chip-select mask register—bank 1 (CSMR1) [p. 10-6]			
0x094	Reserved[1]		Chip-select control register—bank 1 (CSCR1) [p. 10-8]	
0x098	Chip-select address register—bank 2 (CSAR2) [p. 10-6]		Reserved[1]	
0x09C	Chip-select mask register—bank 2 (CSMR2) [p. 10-6]			
0x0A0	Reserved[1]		Chip-select control register—bank 2 (CSCR2) [p. 10-8	
0x0A4	Chip-select address register—bank 3 (CSAR3) [p. 10-6]		Reserved[1]	
0x0A8	Chip-select mask register—bank 3 (CSMR3) [p. 10-6]			
0x0AC	Reserved[1]		Chip-select control register—bank 3 (CSCR3) [p. 10-8]	
0x0B0	Chip-select address register—bank 4 (CSAR4) [p. 10-6]		Reserved[1]	
0x0B4	Chip-select mask register—bank 4 (CSMR4) [p. 10-6]			
0x0B8	Reserved[1]		Chip-select control register—bank 4 (CSCR4) [p. 10-8]	
0x0BC	Chip-select address register—bank 5 (CSAR5) [p. 10-6]		Reserved[1]	
0x0C0	Chip-select mask register—bank 5 (CSMR5) [p. 10-6]			
0x0C4	Reserved		Chip-select control register—bank 5 (CSCR5) [p. 10-8]	
0x0C8	Chip-select address register—bank 6 (CSAR6) [p. 10-6]		Reserved[1]	
0x0CC	Chip-select mask register—bank 6 (CSMR6) [p. 10-6]			
0x0D0	Reserved[1]		Chip-select control register—bank 6 (CSCR6) [p. 10-8]	
0x0D4	Chip-select address register—bank 7 (CSAR7) [p. 10-6]		Reserved[1]	
0x0D8	Chip-select mask register—bank 7 (CSMR7) [p. 10-6]			
0x0DC	Reserved[1]		Chip-select control register—bank 7 (CSCR7) [p. 10-8	

Table A-3. Chip-Select Registers (Continued)

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
MBAR Offset	**[31:24]**	**[23:16]**	**[15:8]**	**[7:0]**
0x080	Chip-select address register—bank 0 (CSAR0) [p. 10-6]		Reserved[1]	
0x084	Chip-select mask register—bank 0 (CSMR0) [p. 10-6]			
0x088	Reserved[1]		Chip-select control register—bank 0 (CSCR0) [p. 10-8]	
0x08C	Chip-select address register—bank 1 (CSAR1) [p. 10-6]		Reserved[1]	
0x090	Chip-select mask register—bank 1 (CSMR1) [p. 10-6]			
0x094	Reserved[1]		Chip-select control register—bank 1 (CSCR1) [p. 10-8]	
0x098	Chip-select address register—bank 2 (CSAR2) [p. 10-6]		Reserved[1]	
0x09C	Chip-select mask register—bank 2 (CSMR2) [p. 10-6]			
0x0A0	Reserved[1]		Chip-select control register—bank 2 (CSCR2) [p. 10-8]	
0x0A4	Chip-select address register—bank 3 (CSAR3) [p. 10-6]		Reserved[1]	
0x0A8	Chip-select mask register—bank 3 (CSMR3) [p. 10-6]			
0x0AC	Reserved[1]		Chip-select control register—bank 3 (CSCR3) [p. 10-8]	
0x0B0	Chip-select address register—bank 4 (CSAR4) [p. 10-6]		Reserved[1]	
0x0B4	Chip-select mask register—bank 4 (CSMR4) [p. 10-6]			
0x0B8	Reserved[1]		Chip-select control register—bank 4 (CSCR4) [p. 10-8]	

[1] Addresses not assigned to a register and undefined register bits are reserved for expansion. Write accesses to these reserved address spaces and reserved register bits have no effect.

Table A-4. DRAM Controller Registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x100	DRAM control register (DCR) [p. 11-3]		Reserved	
0x104	Reserved			
0x108	DRAM address and control register 0 (DACR0) [p. 11-3]			
0x10C	DRAM mask register block 0 (DMR0) [p. 11-3]			
0x110	DRAM address and control register 1 (DACR1) [p. 11-3]			
0x114	DRAM mask register block 1 (DMR1) [p. 11-3]			

Table A-5. General-Purpose Timer Registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x140	Timer 0 mode register (TMR0) [p. 13-3]		Reserved	
0x144	Timer 0 reference register (TRR0) [p. 13-4]		Reserved	
0x148	Timer 0 capture register (TCR0) [p. 13-4]		Reserved	
0x14C	Timer 0 counter (TCN0) [p. 13-5]		Reserved	
0x150	Reserved	Timer 0 event register (TER0) [p. 13-5]	Reserved	
0x180	Timer 1 mode register (TMR1) [p. 13-3]		Reserved	
0x184	Timer 1 reference register (TRR1) [p. 13-4]		Reserved	
0x188	Timer 1 capture register (TCR1) [p. 13-4]		Reserved	
0x18C	Timer 1 counter (TCN1) [p. 13-5]		Reserved	
0x190	Reserved	Timer 1 event register (TER1) [p. 13-5]	Reserved	

Table A-6. UART0 Module Programming Model

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x1C0	UART mode registers[1]—(UMR1n) [p. 14-4], (UMR2n) [p. 14-6]	—		
0x1C4	(Read) UART status registers—(USRn) [p. 14-7]	—		
	(Write) UART clock-select register[1]—(UCSRn) [p. 14-8]	—		
0x1C8	(Read) Do not access[2]	—		
	(Write) UART command registers—(UCRn) [p. 14-9]	—		
0x1CC	(UART/Read) UART receiver buffers—(URBn) [p. 14-11]	—		
	(UART/Write) UART transmitter buffers—(UTBn) [p. 14-11]	—		
0x1D0	(Read) UART input port change registers—(UIPCRn) [p. 14-12]	—		

Table A-6. UART0 Module Programming Model (Continued)

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
	(Write) UART auxiliary control registers[1]—(UACRn) [p. 14-12]	—		
0x1D4	(Read) UART interrupt status registers—(UISRn) [p. 14-13]	—		
	(Write) UART interrupt mask registers—(UIMRn) [p. 14-13]	—		
0x1D8	UART divider upper registers—(UDUn) [p. 14-14]	—		
0x1DC	UART divider lower registers—(UDLn) [p. 14-14]	—		
0x1E0–0x1EC	Do not access[2]	—		
0x1F0	UART interrupt vector register—(UIVRn) [p. 14-15]	—		
0x1F4	(Read) UART input port registers—(UIPn) [p. 14-15]	—		
	(Write) Do not access[2]	—		
0x1F8	(Read) Do not access[2]	—		
	(Write) UART output port bit set command registers—(UOP1n[3]) [p. 14-15]	—		
0x1FC	(Read) Do not access[2]	—		
	(Write) UART output port bit reset command registers—(UOP0n[3]) [p. 14-15]	—		

1 UMR1n, UMR2n, and UCSRn should be changed only after the receiver/transmitter is issued a software reset command. That is, if channel operation is not disabled, undesirable results may occur.

2 This address is for factory testing. Reading this location results in undesired effects and possible incorrect transmission or reception of characters. Register contents may also be changed.

3 Address-triggered commands

Table A-7. UART1 Module Programming Model

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x200	UART mode registers[1]—(UMR1n) [p. 14-4], (UMR2n) [p. 14-6]	—		
0x204	(Read) UART status registers—(USRn) [p. 14-7]	—		
	(Write) UART clock-select register[1]—(UCSRn) [p. 14-8]	—		
0x208	(Read) Do not access[2]	—		
	(Write) UART command registers—(UCRn) [p. 14-9]	—		
0x20C	(UART/Read) UART receiver buffers—(URBn) [p. 14-11]	—		
	(UART/Write) UART transmitter buffers—(UTBn) [p. 14-11]	—		
0x210	(Read) UART input port change registers—(UIPCRn) [p. 14-12]	—		
	(Write) UART auxiliary control registers[1]—(UACRn) [p. 14-12]	—		
0x214	(Read) UART interrupt status registers—(UISRn) [p. 14-13]	—		
	(Write) UART interrupt mask registers—(UIMRn) [p. 14-13]	—		
0x218	UART divider upper registers—(UDUn) [p. 14-14]	—		
0x21C	UART divider lower registers—(UDLn) [p. 14-14]	—		

Table A-7. UART1 Module Programming Model (Continued)

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x220–0x22C	Do not access[2]	—		
0x230	UART interrupt vector register—(UIVRn) [p. 14-15]	—		
0x234	(Read) UART input port registers—(UIPn) [p. 14-15]	—		
	(Write) Do not access[2]	—		
0x238	(Read) Do not access[2]	—		
	(Write) UART output port bit set command registers—(UOP1n[3]) [p. 14-15]	—		
0x23C	(Read) Do not access[2]	—		
	(Write) UART output port bit reset command registers—(UOP0n[3]) [p. 14-15]	—		

1 UMR1n, UMR2n, and UCSRn should be changed only after the receiver/transmitter is issued a software reset command. That is, if channel operation is not disabled, undesirable results may occur.

2 This address is for factory testing. Reading this location results in undesired effects and possible incorrect transmission or reception of characters. Register contents may also be changed.

3 Address-triggered commands

Table A-8. Parallel Port Memory Map

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x244	Parallel port data direction register (PADDR) [p. 15-2]		Reserved	
0x248	Parallel port data register (PADAT) [p. 15-2]		Reserved	

Table A-9. I^2C Interface Memory Map

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x280	I^2C address register (IADR) [p. 8-6]	Reserved		
0x284	I^2C frequency divider register (IFDR) [p. 8-7]	Reserved		

Table A-9. I^2C Interface Memory Map

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x288	I^2C control register (I2CR) [p. 8-8]	Reserved		
0x28C	I^2C status register (I2SR) [p. 8-9]	Reserved		
0x290	I^2C data I/O register (I2DR) [p. 8-10]	Reserved		

Table A-10. DMA Controller Registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x300	Source address register 0 (SAR0) [p. 12-6]			
0x304	Destination address register 0 (DAR0) [p. 12-7]			
0x308	DMA control register 0 (DCR0) [p. 12-8]			
0x30C	Byte count register 0 (BCR24BIT = 0) [1]		Reserved	
0x30C	Reserved	Byte count register 0 (BCR24BIT = 1) [1] (BCR0) [p. 12-7]		
0x310	DMA status register 0 (DSR0) [p. 12-10]	Reserved		
0x314	DMA interrupt vector register 0 (DIVR0) [p. 12-11]	Reserved		
0x340	Source address register 1 (SAR1) [p. 12-6]			
0x344	Destination address register 1 (DAR1) [p. 12-7]			
0x348	DMA control register 1 (DCR1) [p. 12-8]			
0x34C	Byte count register 1 (BCR24BIT = 0) [1]		Reserved	
0x34C	Reserved	Byte count register 1 (BCR24BIT = 1) [1] (BCR1) [p. 12-7]		
0x350	DMA status register 1 (DSR1) [p. 12-10]	Reserved		
0x354	DMA interrupt vector register 1 (DIVR1) [p. 12-11]	Reserved		
0x380	Source address register 2 (SAR2) [p. 12-6]			
0x384	Destination address register 2 (DAR2) [p. 12-7]			
0x388	DMA control register 2 (DCR2) [p. 12-8]			
0x38C	Byte count register 2 (BCR24BIT = 0) [1]		Reserved	
0x38C	Reserved	Byte count register 2 (BCR24BIT = 1) [1] (BCR2) [p. 12-7]		
0x390	DMA status register 2 (DSR2) [p. 12-10]	Reserved		

Table A-10. DMA Controller Registers (Continued)

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x394	DMA interrupt vector register 2 (DIVR2) [p. 12-11]	Reserved		
0x3C0	Source address register 3 (SAR3) [p. 12-6]			
0x3C4	Destination address register 3 (DAR3) [p. 12-7]			
0x3C8	DMA control register 3 (DCR3) [p. 12-8]			
0x3CC	Byte count register 3 (BCR24BIT = 0) [1]		Reserved	
0x3CC	Reserved	Byte count register 3 (BCR24BIT = 1) [1] (BCR3) [p. 12-7]		
0x3D0	DMA status register 3 (DSR3) [p. 12-10]	Reserved		
0x3D4	DMA interrupt vector register 3 (DIVR3) [p. 12-11]	Reserved		

[1] On the 0H55J and 1H55J revisions of the MCF5307, the byte count register of the DMA channels can accommodate only 16 bits. However, on the newest revision of the MCF5307, an expanded 24-bit byte count range provides greater flexibility. For this reason, the position of the byte count register (BCR) in the memory map depends on whether a 16- or 24-bit byte counter is chosen. The selection is made by programming MPARK[BCR24BIT] in the SIM module.

In the new MCF5307, the 24-bit byte count can be selected by setting BCR24BIT = 1, making DCR[AT] available. The AT bit selects whether the DMA channels assert an acknowledge during the entire transfer or only at the final transfer of a DMA transaction.

New applications should take advantage of the full range of the 24-bit byte counter, including the AT bit. The 16-bit byte count option (BCR24BIT = 0) is kept to retain compatibility with older revisions of the MCF5307.