Chapter 10
Chip-Select Module

This chapter describes the MCF5307 chip-select module, including the operation and programming model of the chip-select registers, which include the chip-select address, mask, and control registers.

10.1 Overview

The following list summarizes the key chip-select features:

- Eight independent, user-programmable chip-select signals ($\overline{CS}$[7:0]) that can interface with SRAM, PROM, EPROM, EEPROM, Flash, and peripherals
- Address masking for 64-Kbyte to 4-Gbyte memory block sizes
- Programmable wait states and port sizes
- External master access to chip selects

10.2 Chip-Select Module Signals

Table 10-1 lists signals used by the chip-select module.

Table 10-1. Chip-Select Module Signals

Signal	Description
Chip Selects ($\overline{CS}$[7:0])	Each $\overline{CSn}$ can be independently programmed for an address location as well as for masking, port size, read/write burst-capability, wait-state generation, and internal/external termination. Only $\overline{CS0}$ is initialized at reset when it acts as a global chip select that allows boot ROM to be at any defined address space. Port size and termination (internal versus external) and byte enables for $\overline{CS0}$ are configured by the logic levels of D[7:5] when $\overline{RSTI}$ negates.
Output Enable ($\overline{OE}$)	Interfaces to memory or to peripheral devices and enables a read transfer. It is asserted and negated on the falling edge of the clock. $\overline{OE}$ is asserted only when one of the chip selects matches for the current address decode.
Byte Enables/ Byte Write Enables ($\overline{BE}$[3:0]/ $\overline{BWE}$[3:0])	These multiplexed signals are individually programmed through the byte enable mode bit, CSCRn[BEM], described in Section 10.4.1.3, “Chip-Select Control Registers (CSCR0–CSCR7).” These generated signals provide byte data select signals, which are decoded from the transfer size, A1, and A0 signals in addition to the programmed port size and burstability of the memory accessed, as Table 10-2 shows.

Table 10-2 shows the interaction of the byte enable/byte-write enables with related signals.

Table 10-2. Byte Enables/Byte Write Enable Signal Settings

Transfer Size	Port Size	A1	A0	$\overline{\text{BE0/BWE0}}$	$\overline{\text{BE1/BWE1}}$	$\overline{\text{BE2/BWE2}}$	$\overline{\text{BE3/BWE3}}$
				D[31:24]	D[23:16]	D[15:8]	D[7:0]
Byte	8-bit	0	0	0	1	1	1
		0	1	0	1	1	1
		1	0	0	1	1	1
		1	1	0	1	1	1
	16-bit	0	0	0	1	1	1
		0	1	1	0	1	1
		1	0	0	1	1	1
		1	1	1	0	1	1
	32-bit	0	0	0	1	1	1
		0	1	1	0	1	1
		1	0	1	1	0	1
		1	1	1	1	1	0
Word	8-bit	0	0	0	1	1	1
		0	1	0	1	1	1
		1	0	0	1	1	1
		1	1	0	1	1	1
	16-bit	0	0	0	0	1	1
		1	0	0	0	1	1
	32-bit	0	0	0	0	1	1
		1	0	1	1	0	0
Longword	8-bit	0	0	0	1	1	1
		0	1	0	1	1	1
		1	0	0	1	1	1
		1	1	0	1	1	1
	16-bit	0	0	0	0	1	1
		1	0	0	0	1	1
	32-bit	0	0	0	0	0	0
Line	8-bit	0	0	0	1	1	1
		0	1	0	1	1	1
		1	0	0	1	1	1
		1	1	0	1	1	1
	16-bit	0	0	0	0	1	1
		1	0	0	0	1	1
	32-bit	0	0	0	0	0	0

10.3 Chip-Select Operation

Each chip select has a dedicated set of the following registers for configuration and control.

- Chip-select address registers (CSAR*n*) control the base address space of the chip select. See Section 10.4.1.1, “Chip-Select Address Registers (CSAR0–CSAR7).”

- Chip-select mask registers (CSMR*n*) provide 16-bit address masking and access control. See Section 10.4.1.2, “Chip-Select Mask Registers (CSMR0–CSMR7).”
- Chip-select control registers (CSCR*n*) provide port size and burst capability indication, wait-state generation, and automatic acknowledge generation features. See Section 10.4.1.3, “Chip-Select Control Registers (CSCR0–CSCR7).”

Each $\overline{\text{CS}n}$ can assert during specific CPU space accesses such as interrupt-acknowledge cycles and each can be accessed by an external master. $\overline{\text{CS0}}$ is a global chip select after reset and provides relocatable boot ROM capability.

10.3.1 General Chip-Select Operation

When a bus cycle is initiated, the MCF5307 first compares its address with the base address and mask configurations programmed for chip selects 0–7 (configured in CSCR0–CSCR7) and DRAM block 0 and 1 address and control registers (configured in DACR0 and DACR1). If the driven address matches a programmed chip select or DRAM block, the appropriate chip select is asserted or the DRAM block is selected using the specifications programmed in the respective configuration register. Otherwise, the following occurs:

- If the address and attributes do not match in CSCR or DACR, the MCF5307 runs an external burst-inhibited bus cycle with a default of external termination on a 32-bit port.
- Should an address and attribute match in multiple CSCRs, the matching chip-select signals are driven; however, the MCF5307 runs an external burst-inhibited bus cycle with external termination on a 32-bit port.
- Should an address and attribute match both DACRs or a DACR and a CSCR, the operation is undefined.

Table 10-3 shows the type of access as a function of match in the CSCRs and DACRs.

Table 10-3. Accesses by Matches in CSCRs and DACRs

Number of CSCR Matches	Number of DACR Matches	Type of Access
0	0	External
1	0	Defined by CSCR
Multiple	0	External, burst-inhibited, 32-bit
0	1	Defined by DACRs
1	1	Undefined
Multiple	1	Undefined
0	Multiple	Undefined
1	Multiple	Undefined
Multiple	Multiple	Undefined

10.3.1.1 8-, 16-, and 32-Bit Port Sizing

Static bus sizing is programmable through the port size bits, CSCR[PS]. See Section 10.4.1.3, “Chip-Select Control Registers (CSCR0–CSCR7).” Figure 10-1 shows the correspondence between data byte lanes and the external chip-select memory. Note that all lanes are driven, although unused lines are undefined.

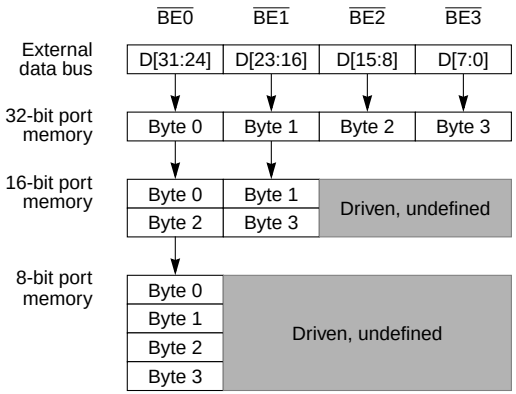

Figure 10-1. Connections for External Memory Port Sizes

10.3.1.2 Global Chip-Select Operation

$\overline{CS0}$, the global (boot) chip select, allows address decoding for boot ROM before system initialization. Its operation differs from other external chip-select outputs after system reset.

After system reset, $\overline{CS0}$ is asserted for every external access. No other chip-select can be used until the valid bit, CSMR0[V], is set, at which point $\overline{CS0}$ functions as configured and $\overline{CS}$[7:1] can be used. At reset, the port size and automatic acknowledge functions of the global chip-select are determined by the logic levels of the inputs on D[7:5]. Table 10-4 and Table 10-5list the various reset encodings for the configuration signals multiplexed with D[7:5].

Table 10-4. D7/AA, Automatic Acknowledge of Boot $\overline{CS0}$

D7/AA	Boot $\overline{CS0}$ AA Configuration at Reset
0	Disabled
1	Enable with 15 wait states

Provided the required address range is in the chip-select address register (CSAR0), $\overline{CS0}$ can

Table 10-5. D[6:5]/PS[1:0], Port Size of Boot $\overline{CS0}$

D[6:5]/PS[1:0]	Boot $\overline{CS0}$ Port Size at Reset
00	32-bit port
01	8-bit port
1x	16-bit port

be programmed to continue decoding for a range of addresses after the CSMR0[V] is set, after which the global chip-select can be restored only by a system reset.

10.4 Chip-Select Registers

Table 10-6Table 10-6 is the chip-select register memory map. Reading reserved locations returns zeros.

Table 10-6. Chip-Select Registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x080	Chip-select address register—bank 0 (CSAR0) [p. 10-6]		Reserved[1]	
0x084	Chip-select mask register—bank 0 (CSMR0) [p. 10-6]			
0x088	Reserved[1]		Chip-select control register—bank 0 (CSCR0) [p. 10-8]	
0x08C	Chip-select address register—bank 1 (CSAR1) [p. 10-6]		Reserved[1]	
0x090	Chip-select mask register—bank 1 (CSMR1) [p. 10-6]			
0x094	Reserved[1]		Chip-select control register—bank 1 (CSCR1) [p. 10-8]	
0x098	Chip-select address register—bank 2 (CSAR2) [p. 10-6]		Reserved[1]	
0x09C	Chip-select mask register—bank 2 (CSMR2) [p. 10-6]			
0x0A0	Reserved[1]		Chip-select control register—bank 2 (CSCR2) [p. 10-8]	
0x0A4	Chip-select address register—bank 3 (CSAR3) [p. 10-6]		Reserved[1]	
0x0A8	Chip-select mask register—bank 3 (CSMR3) [p. 10-6]			
0x0AC	Reserved[1]		Chip-select control register—bank 3 (CSCR3) [p. 10-8]	
0x0B0	Chip-select address register—bank 4 (CSAR4) [p. 10-6]		Reserved[1]	
0x0B4	Chip-select mask register—bank 4 (CSMR4) [p. 10-6]			
0x0B8	Reserved[1]		Chip-select control register—bank 4 (CSCR4) [p. 10-8]	
0x0BC	Chip-select address register—bank 5 (CSAR5) [p. 10-6]		Reserved[1]	
0x0C0	Chip-select mask register—bank 5 (CSMR5) [p. 10-6]			
0x0C4	Reserved		Chip-select control register—bank 5 (CSCR5) [p. 10-8]	
0x0C8	Chip-select address register—bank 6 (CSAR6) [p. 10-6]		Reserved[1]	
0x0CC	Chip-select mask register—bank 6 (CSMR6) [p. 10-6]			
0x0D0	Reserved[1]		Chip-select control register—bank 6 (CSCR6) [p. 10-8]	
0x0D4	Chip-select address register—bank 7 (CSAR7) [p. 10-6]		Reserved[1]	

Table 10-6. Chip-Select Registers (Continued)

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x0D8	Chip-select mask register—bank 7 (CSMR7) [p. 10-6]			
0x0DC	Reserved[1]		Chip-select control register—bank 7 (CSCR7) [p. 10-8]	

[1] Addresses not assigned to a register and undefined register bits are reserved for expansion. Write accesses to these reserved address spaces and reserved register bits have no effect.

NOTE:

External masters cannot access MCF5307 on-chip memories or MBAR, but can access any of the chip-select module registers.

10.4.1 Chip-Select Module Registers

The chip-select module is programmed through the chip select address registers (CSAR0–CSAR7), chip select mask registers (CSMR0–CSMR7), and the chip select control registers (CSCR0–CSCR7).

10.4.1.1 Chip-Select Address Registers (CSAR0–CSAR7)

Chip select address registers, Figure 10-2, specify the chip select base addresses.

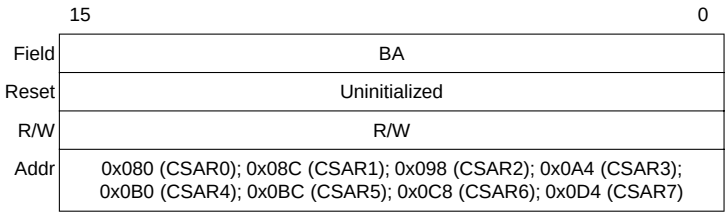

Figure 10-2. Chip Select Address Registers (CSAR0–CSAR7)

Table 10-7 describes CSAR[BA].

Table 10-7. CSAR*n* Field Description

Bits	Name	Description
15–0	BA	Base address. Defines the base address for memory dedicated to chip select $\overline{CS}$[7:0]. BA is compared to bits 31–16 on the internal address bus to determine if chip-select memory is being accessed.

10.4.1.2 Chip-Select Mask Registers (CSMR0–CSMR7)

The chip select mask registers, Figure 10-3, are used to specify the address mask and allowable access types for the respective chip selects.

	31 16	15 9	8	7	6	5	4	3	2	1	0
Field	BAM	—	WP	—	AM	C/I	SC	SD	UC	UD	V
Reset	Unitialized										0
R/W	R/W										
Addr	0x084 (CSMR0); 0x090 (CSMR1); 0x09C (CSMR2); 0x0A8 (CSMR3); 0x0B4 (CSMR4); 0x0C0 (CSMR5); 0x0CC (CSMR6); 0x0D8 (CSMR7)										

Figure 10-3. Chip Select Mask Registers (CSMR*n*)

Table 10-8 describes CSMR fields.

Table 10-8. CSMR*n* Field Descriptions

Bits	Name	Description
31–16	BAM	Base address mask. Defines the chip select block by masking address bits. Setting a BAM bit causes the corresponding CSAR bit to be ignored in the decode. 0 Corresponding address bit is used in chip-select decode. 1 Corresponding address bit is a don't care in chip-select decode. The block size for $\overline{CS}$[7:0] is 2^n; n = (number of bits set in respective CSMR[BAM]) + 16. So, if CSAR0 = 0x0000 and CSMR0[BAM] = 0x0008, $\overline{CS0}$ would address two discontinuous 64-Kbyte memory blocks: one from 0x0000–0xFFFF and one from 0x8_0000–0x8_FFFF. Likewise, for $\overline{CS0}$ to access 32 Mbytes of address space starting at location 0x0, $\overline{CS1}$ must begin at the next byte after $\overline{CS0}$ for a 16-Mbyte address space. Then CSAR0 = 0x0000, CSMR0[BAM] = 0x01FF, CSAR1 = 0x0200, and CSMR1[BAM] = 0x00FF.
8	WP	Write protect. Controls write accesses to the address range in the corresponding CSAR. Attempting to write to the range of addresses for which CSARn[WP] = 1 results in the appropriate chip select not being selected. No exception occurs. 0 Both read and write accesses are allowed. 1 Only read accesses are allowed.
7	—	Reserved, should be cleared.
6	AM	Alternate master. When AM = 0 during an external master or DMA access, SC, SD, UC, and UD are don't cares in the chip-select decode.
5–1	C/I, SC, SD, UC, UD	Address space mask bits. These bits determine whether the specified accesses can occur to the address space defined by the BAM for this chip select. C/I CPU space and interrupt acknowledge cycle mask SC Supervisor code address space mask SD Supervisor data address space mask UC User code address space mask UD User data address space mask 0 The address space assigned to this chip select. is available to the specified access type. 1 The address space assigned to this chip select. is not available (masked) to the specified access type. If this address space is accessed, chip select is not activated and a regular external bus cycle occurs. Note that if if AM = 0, SC, SD, UC, and UD are ignored in the chip select decode on external master or DMA access.
0	V	Valid bit. Indicates whether the corresponding CSAR, CSMR, and CSCR contents are valid. Programmed chip selects do not assert until V is set (except for $\overline{CS0}$, which acts as the global chip select). Reset clears each CSMRn[V]. 0 Chip select invalid 1 Chip select valid

10.4.1.3 Chip-Select Control Registers (CSCR0–CSCR7)

Each chip-select control register, Figure 10-4, controls the auto acknowledge, external master support, port size, burst capability, and activation of each chip select. Note that to support the global chip select, $\overline{CS0}$, the CSCR0 reset values differ from the other CSCRs. $\overline{CS0}$ allows address decoding for boot ROM before system initialization.

	15 14	13 10	9	8	7	6	5	4	3	2 0
Field	—	WS	—	AA	PS1	PS0	BEM	BSTR	BSTW	—
Reset: CSCR0	—	11_11	—	D7	D6	D5	—	—		
Reset: Other CSCRs	Unitialized									
R/W	R/W									
Address	0x08A (CSCR0); 0x096 (CSCR1); 0x0A2 (CSCR2); 0x0AE (CSCR3); 0x0BA (CSCR4); 0x0C6 (CSCR5); 0x0D2 (CSCR6); 0x0DE (CSCR7)									

Figure 10-4. Chip-Select Control Registers (CSCR0–CSCR7)

Table 10-9 describes CSCR*n* fields.

Table 10-9. CSCR*n* Field Descriptions

Bits	Name	Description
15–14	—	Reserved, should be cleared.
13–10	WS	Wait states. The number of wait states inserted before an internal transfer acknowledge is generated (WS = 0 inserts zero wait states, WS = 0xF inserts 15 wait states). If AA = 0, $\overline{TA}$ must be asserted by the external system regardless of the number of wait states generated. In that case, the external transfer acknowledge ends the cycle. An external $\overline{TA}$ supersedes the generation of an internal $\overline{TA}$.
9	—	Reserved, should be cleared.
8	AA	Auto-acknowledge enable. Determines the assertion of the internal transfer acknowledge for accesses specified by the chip-select address. 0 No internal $\overline{TA}$ is asserted. Cycle is terminated externally. 1 Internal $\overline{TA}$ is asserted as specified by WS. Note that if AA = 1 for a corresponding $\overline{CS}$n and the external system asserts an external $\overline{TA}$ before the wait-state countdown asserts the internal $\overline{TA}$, the cycle is terminated. Burst cycles increment the address bus between each internal termination.
7–6	PS	Port size. Specifies the width of the data associated with each chip select. It determines where data is driven during write cycles and where data is sampled during read cycles. See Section 10.3.1.1, “8-, 16-, and 32-Bit Port Sizing.” 00 32-bit port size. Valid data sampled and driven on D[31:0] 01 8-bit port size. Valid data sampled and driven on D[31:24] 1x 16-bit port size. Valid data sampled and driven on D[31:16]
5	BEM	Byte enable mode. Specifies the byte enable operation. Certain SRAMs have byte enables that must be asserted during reads as well as writes. BEM can be set in the relevant CSCR to provide the appropriate mode of byte enable in support of these SRAMs. 0 Neither $\overline{BE}$ nor $\overline{BWE}$ is asserted for read. $\overline{BWE}$ is generated for data write only. 1 $\overline{BE}$ is asserted for read; $\overline{BWE}$ is asserted for write.
4	BSTR	Burst read enable. Specifies whether burst reads are used for memory associated with each $\overline{CS}$n. 0 Data exceeding the specified port size is broken into individual, port-sized non-burst reads. For example, a longword read from an 8-bit port is broken into four 8-bit reads. 1 Enables data burst reads larger than the specified port size, including longword reads from 8- and 16-bit ports, word reads from 8-bit ports, and line reads from 8-, 16-, and 32-bit ports.

Table 10-9. CSCR*n* Field Descriptions

Bits	Name	Description
3	BSTW	Burst write enable. Specifies whether burst writes are used for memory associated with each $\overline{CS}$n. 0 Break data larger than the specified port size into individual port-sized, non-burst writes. For example, a longword write to an 8-bit port takes four byte writes. 1 Enables burst write of data larger than the specified port size, including longword writes to 8 and 16-bit ports, word writes to 8-bit ports and line writes to 8-, 16-, and 32-bit ports.
2–0	—	Reserved, should be cleared.

10.4.1.4 Code Example

The code below provides an example of how to initialize the chip-selects. Only chip selects 0, 1, 2, and 3 are programmed here; chip selects 4, 5, 6, and 7 are left invalid. MBARx defines the base of the module address space.

```
CSAR0 EQU MBARx+0x080   ;Chip select 0 address register
CSMR0 EQU MBARx+0x084   ;Chip select 0 mask register
CSCR0 EQU MBARx+0x08A   ;Chip select 0 control register

CSAR1 EQU MBARx+0x08C   ;Chip select 1 address register
CSMR1 EQU MBARx+0x090   ;Chip select 1 mask register
CSCR1 EQU MBARx+0x096   ;Chip select 1 control register

CSAR2 EQU MBARx+0x098   ;Chip select 2 address register
CSMR2 EQU MBARx+0x09C   ;Chip select 2 mask register
CSCR2 EQU MBARx+0x0A2   ;Chip select 2 control register

CSAR3 EQU MBARx+0x0A4   ;Chip select 3 address register
CSMR3 EQU MBARx+0x0A8   ;Chip select 3 mask register
CSCR3 EQU MBARx+0x0AE   ;Chip select 3 control register

CSAR4 EQU MBARx+0x0B0   ;Chip select 4 address register
CSAR4 EQU MBARx+0x0B4   ;Chip select 4 mask register
CSMR4 EQU MBARx+0x0BA   ;Chip select 4 control register

CSAR5 EQU MBARx+0x0BC   ;Chip select 5 address register
CSMR5 EQU MBARx+0x0C0   ;Chip select 5 mask register
CSCR5 EQU MBARx+0x0C6   ;Chip select 5 control register

CSAR6 EQU MBARx+0x0C8   ;Chip select 6 address register
CSMR6 EQU MBARx+0x0CC   ;Chip select 6 mask register
CSCR6 EQU MBARx+0x0D2   ;Chip select 6 control register

CSAR7 EQU MBARx+0x0D4   ;Chip select 7 address register
CSMR7 EQU MBARx+0x0D8   ;Chip select 7 mask register
CSCR7 EQU MBARx+0x0DE   ;Chip select 7 control register

; All other chip selects should be programmed and made valid before global
; chip select is de-activated by validating CS0

; Program Chip Select 3 Registers
move.w  #0x0040,D0      ;CSAR3 base address 0x00400000
move.w  D0,CSAR3

move.w  #0x00A0,D0      ;CSCR3 = no wait states, AA=0, PS=16-bit, BEM=1,
move.w  D0,CSCR3        ;BSTR=0, BSTW=0

move.l #0x001F016B,D0   ;Address range from 0x00400000 to 0x005FFFFF
move.l D0,CSMR3         ;WP,EM,C/I,SD,UD,V=1; SC,UC=0

; Program Chip Select 2 Registers

move.w  #0x0020,D0      ;CSAR2 base address 0x00200000 (to 0x003FFFFF)
```

```
move.w  D0,CSAR2

move.w  #0x0538,D0      ;CSCR2 = 1 wait state, AA=1, PS=32-bit, BEM=1,
move.w  D0,CSCR2        ;BSTR=1, BSTW=1

move.l  #0x001F0001,D0  ;Address range from 0x00200000 to 0x003FFFFF
move.l  D0,CSMR2        ;WP,EM,C/I,SC,SD,UC,UD=0; V=1

; Program Chip Select 1 Registers

move.w  #0x0000,D0      ;CSAR1 base addresses 0x00000000 (to 0x001FFFFF)
move.w  D0,CSAR1        ;and 0x80000000 (to 0x801FFFFF)

move.w  #0x09B0,D0      ;CSCR1 = 2 wait states, AA=1, PS=16-bit, BEM=1,
move.w  D0,CSCR1        ;BSTR=1, BSTW=0

move.l  #0x801F0001,D0  ;Address range from 0x00000000 to 0x001FFFFF and
move.l  D0,CSMR1        ;0x80000000 to 0x801FFFFF
                        ;WP, EM, C/I, SC, SD, UC, UD=0, V=1

; Program Chip Select 0 Registers

move.w  #0x0080,D0      ;CSAR0 base address 0x00800000 (to 0x009FFFFF)
move.w  D0,CSAR0

move.w  #0x0D80,D0      ;CSCR0 = three wait states, AA=1, PS=16-bit, BEM=0,
move.w  D0,CSCR0        ;BSTR=0, BSTW=0

; Program Chip Select 0 Mask Register (validate chip selects)

move.l  #0x001F0001,D0  ;Address range from 0x00800000 to 0x009FFFFF
move.l  D0,CSMR0        ;WP,EM,C/I,SC,SD,UC,UD=0; V=1
```