Chapter 20
Electrical Specifications

This chapter describes the AC and DC electrical specifications and thermal characteristics for the MCF5307. Note that this information was correct at the time this book was published. As process technologies improve, there is a likelihood that this information may change. To confirm that this is the latest information, see Motorola's ColdFire webpage, http://www.motorola.com/coldfire.

20.1 General Parameters

Table 20-1 lists maximum and minimum ratings for supply and operating voltages and storage temperature. Operating outside of these ranges may cause erratic behavior or damage to the processor.

Table 20-1. Absolute Maximum Ratings

Rating	Symbol	Value	Units
Supply voltage	V_{cc}	-0.3 to +4.0	V
Maximum operating voltage	V_{cc}	+3.6	V
Minimum operating voltage	V_{cc}	+3.0	V
Input voltage	V_{in}	-0.5 to +5.5	V
Storage temperature range	T_{stg}	-55 to +150	^{o}C

Table 20-2 lists junction and ambient operating temperatures.

Table 20-2. Operating Temperatures

Characteristic	Symbol	Value	Units
Maximum operating junction temperature	T_j	105	^{o}C
Maximum operating ambient temperature	T_{Amax}	70 [1]	^{o}C
Minimum operating ambient temperature	T_{Amin}	0	^{o}C

[1] This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature lies within the specified range.

Table 20-3 lists DC electrical operating temperatures. This table is based on an operating

voltage of Vcc = 3.3 Vdc ± 0.3 Vdc.

Table 20-3. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
Operation voltage range	V_{cc}	3.0	3.6	V
Input high voltage	V_{IH}	2.0	3.6	V
Input low voltage	V_{IL}	-0.5	0.8	V
Input signal undershoot	—	—	0.8	V
Input signal overshoot	—	—	0.8	V
Input leakage current @ 0.5/2.4 V during normal operation	I_{in}	—	20	µA
High impedance (three-state) leakage current @ 0.5/2.4 V during normal operation	I_{TSI}	—	20	µA
Signal low input current, V_{IL} = 0.8 V [1]	I_{IL}	0	1	mA
Signal high input current, V_{IH} = 2.0 V [1]	I_{IH}	0	1	mA
Output high voltage I_{OH} = 6 mA [2], 12 mA [3]	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 6 mA [2], 12 mA [3]	V_{OL}	—	0.5	V
Load capacitance (all outputs)	C_L	—	50	pF
Capacitance [4], V_{in} = 0 V, f = 1 MHz	C_{IN}	—	10	pF

1 $\overline{\text{BKPT}}$/TMS, DSI/TDI, DSCLK/$\overline{\text{TRST}}$

2 D[31:0], A[23:0], PP[15:0],$\overline{\text{TS}}$, $\overline{\text{TA}}$, SIZ[1:0], R/$\overline{\text{W}}$, $\overline{\text{BR}}$, $\overline{\text{BD}}$, $\overline{\text{RSTO}}$, $\overline{\text{AS}}$, $\overline{\text{CS}}$[7:0], $\overline{\text{BE}}$[3:0], $\overline{\text{OE}}$, PSTCLK, PST[3:0], DDATA[3:0], DSO, TOUT[1:0], SCL, SDA, $\overline{\text{RTS}}$[1:0], TXD[1:0]

3 BCLKO, $\overline{\text{RAS}}$[1:0], $\overline{\text{CAS}}$[3:0], $\overline{\text{DRAMW}}$, SCKE, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$

4 Capacitance C_{IN} is periodically sampled rather than 100% tested.

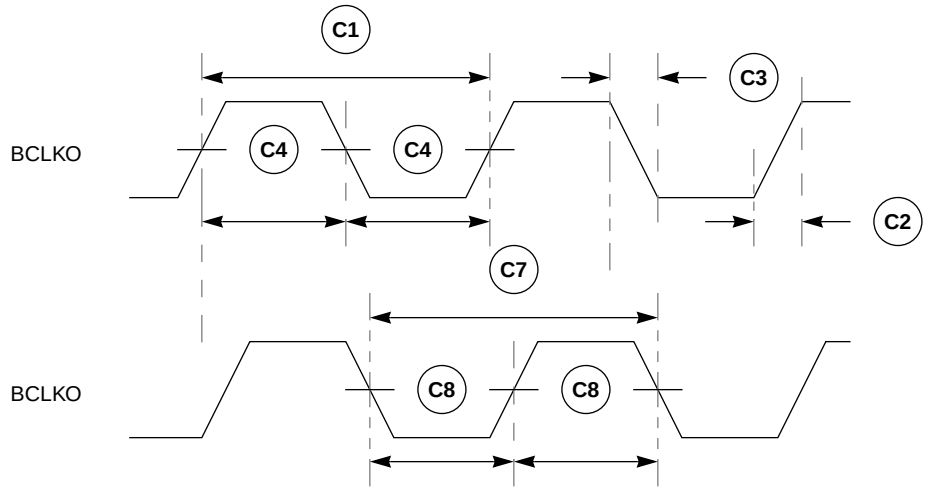
20.2 Clock Timing Specifications

Table 20-4 lists specifications for the clock timing parameters shown in Figure 20-1 and Figure 20-2.

Table 20-4. Clock Timing Specification

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
C1	CLKIN cycle time	30	—	22	—	nS
C2	CLKIN rise time (0.5V to 2.4 V)	—	5	—	5	nS
C3	CLKIN fall time (2.4V to 0.5 V)	—	5	—	5	nS
C4	CLKIN duty cycle (at 1.5 V)	40	60	40	60	%
C5	PSTCLK cycle time	15	—	11	—	nS
C6	PSTCLK duty cycle (at 1.5 V)	40	60	40	60	%
C7	BCLKO cycle time	30	—	22	—	nS
C8	BCLKO duty cycle (at 1.5 V)	45	55	45	55	%

Figure 20-1 shows timings for the parameters listed in Table 20-4.



Note: Input and output AC timing specifications are measured to BCLKO with a 50-pF load capacitance (not including pin capacitance).

Figure 20-1. Clock Timing

Figure 20-2 shows PSTCLK timings for parameters listed in Table 20-4.

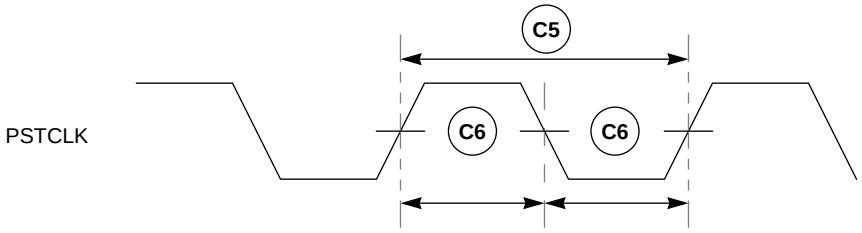


Figure 20-2. PSTCLK Timing

20.3 Input/Output AC Timing Specifications

Table 20-5 lists specifications for parameters shown in Figure 20-3 and Figure 20-4. Note that inputs $\overline{\text{IRQ}}$[7,5,3,1], $\overline{\text{BKPT}}$, and $\overline{\text{AS}}$ are synchronized internally; that is, the logic level is validated if the value does not change for two consecutive rising BCLKO edges. Setup and hold times must be met only if recognition on a particular clock edge is required.

Table 20-5. Input AC Timing Specification

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
B1 [1]	Valid to BCLKO rising (setup)	7.5	—	5.5	—	nS
B2 [1]	BCLKO rising to invalid (hold)	3	—	2	—	nS
B3 [2]	Valid to BCLKO falling (setup)	7.5	—	5.5	—	nS
B4 [2]	BCLKO falling to invalid (hold)	3	—	2	—	nS

Table 20-5. Input AC Timing Specification

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
B5 [3]	BCLKO to input high impedance	—	2	—	2	Bus clock
B6	BCLKO to EDGESEL delay	0	7.5	0	5.5	nS

1 Inputs: $\overline{BG}$, $\overline{TA}$, A[23:0], PP[15:0], SIZ[1:0], R/$\overline{W}$, $\overline{TS}$, EDGESEL, D[31:0], $\overline{IRQ}$[7,5,3,1], and $\overline{BKPT}$

2 Inputs: $\overline{AS}$

3 Inputs: D[31:0]

Table 20-6 lists specifications for timings in Figure 20-3, Figure 20-4, and Figure 20-10. Although output signals that share a specification number have approximately the same timing, due to loading differences, they do not necessarily change at the same time. However, they have similar timings; that is, minimum and maximum times are not mixed.

Table 20-6. Output AC Timing Specification

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
B10 [1,2,3]	BCLKO rising to valid	—	15	—	11	nS
B11 [1,2,3,4]	BCLKO rising to invalid (hold)	1	—	1	—	nS
B11a [1,2,3,5]	BCLKO rising to invalid (hold)	0.5	—	0.5	—	
B12 [6,7]	BCLKO to high impedance (three-state)	—	15	—	11	nS
B13 [8,2,3]	BCLKO rising to valid	—	15	—	11	nS
B14 [8,2,3]	BCLKO rising to invalid (hold)	3	—	2	—	nS
B15 [2,3]	EDGESEL to valid	—	18.5	—	13.5	nS
B16 [2,3]	EDGESEL to invalid (hold)	3	—	2	—	nS
H1	$\overline{HIZ}$ to high impedance	—	60	—	60	nS
H2	$\overline{HIZ}$ to low Impedance	—	60	—	60	nS

1 Outputs that only change on rising edge of BCLKO: $\overline{RSTO}$, $\overline{TS}$, $\overline{BR}$, $\overline{BD}$, $\overline{TA}$, R/$\overline{W}$, SIZ[1:0], PP[7:0] (and PP[15:8] when configured as parallel port outputs).

2 Outputs that can change on either BCLKO edge depending only upon EDGESEL: D[31:0], A[23:0], SCKE, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{DRAMW}$ (and PP[15:8] when individually configured as address outputs).

3 Outputs that can change on either BCLKO edge depending only upon EDGESEL: D[31:0], A[23:0], SCKE, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{DRAMW}$ (and PP[15:8] when individually configured as address outputs).

4 Applies to D[31:0], A[23:0], $\overline{RSTO}$, $\overline{TS}$, $\overline{BR}$, $\overline{BD}$, $\overline{TA}$, R/$\overline{W}$, SIZ[1:0], PP[7:0] (and PP[15:8] when configured as parallel port outputs).

5 Applies to $\overline{RAS}$[1:0], $\overline{CAS}$[1:0], SCKE, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{DRAMW}$

6 High Impedance (three-state): D[31:0]

7 Outputs that transition to high-impedance due to bus arbitration: A[23:0], R/$\overline{W}$, SIZ[1:0], $\overline{TS}$, $\overline{AS}$, $\overline{TA}$, (and PP[15:0] when individually configured as address outputs)

8 Outputs that only change on falling edge of BCLKO: $\overline{AS}$, $\overline{CS}$[7:0], $\overline{BE}$[3:0], $\overline{OE}$

Note that these figures show two representative bus operations and do not attempt to show all cases. For explanations of the states, S0–S5, see Section 18.4, “Data Transfer

Operation.” Note that Figure 20-4 does not show all signals that apply to each timing specification. See the previous tables for a complete listing.

Figure 20-3 shows AC timings for normal read and write bus cycles.

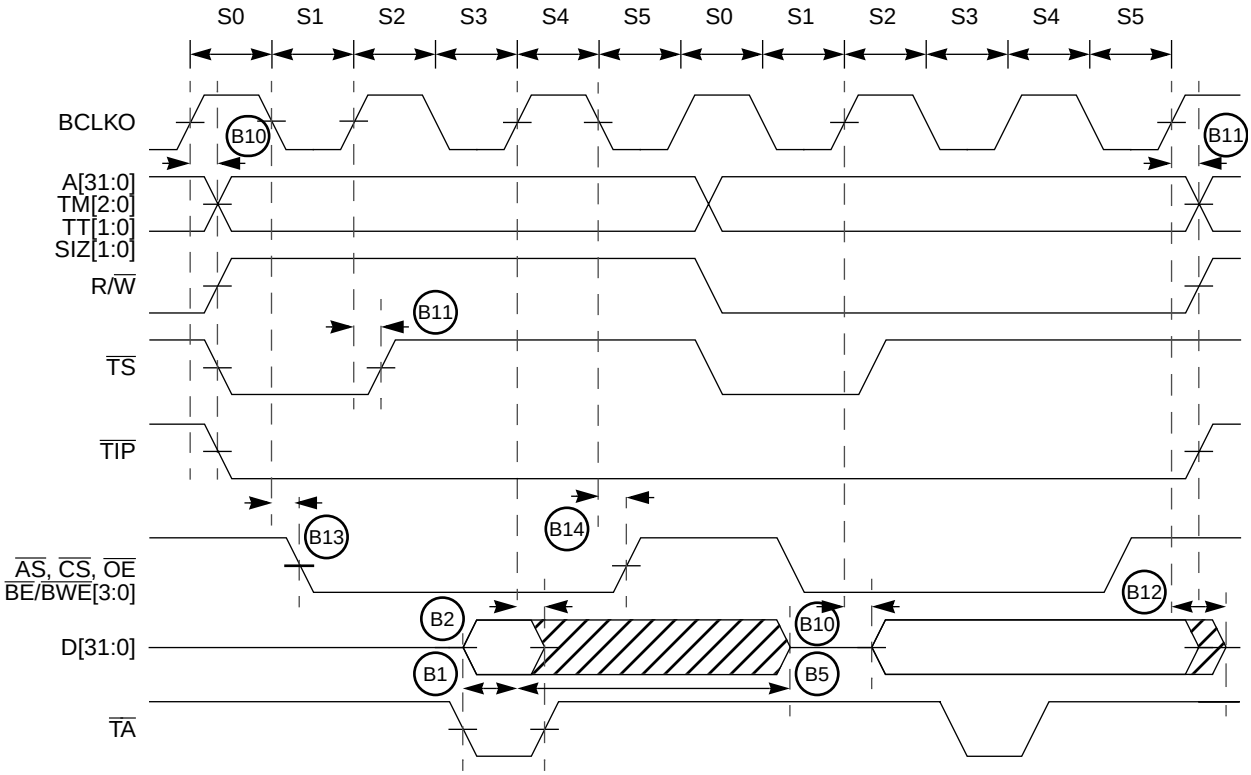


Figure 20-3. AC Timings—Normal Read and Write Bus Cycles

Figure 20-4 shows timings for a read cycle with EDGESEL tied to buffered BCLKO.

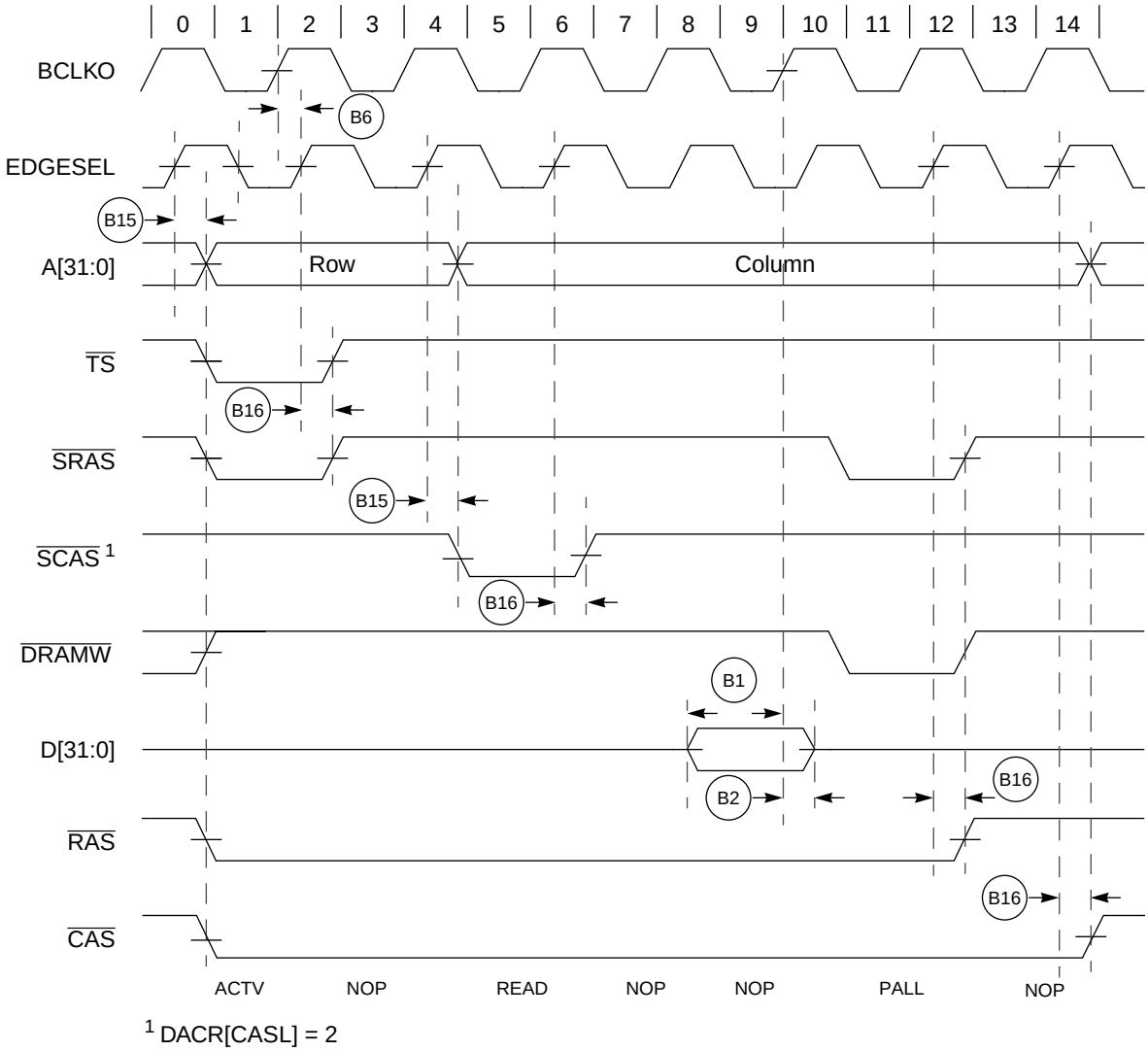


Figure 20-4. SDRAM Read Cycle with EDGESEL Tied to Buffered BCLKO

Figure 20-5 shows an SDRAM write cycle with EDGESEL tied to buffered BCLKO.

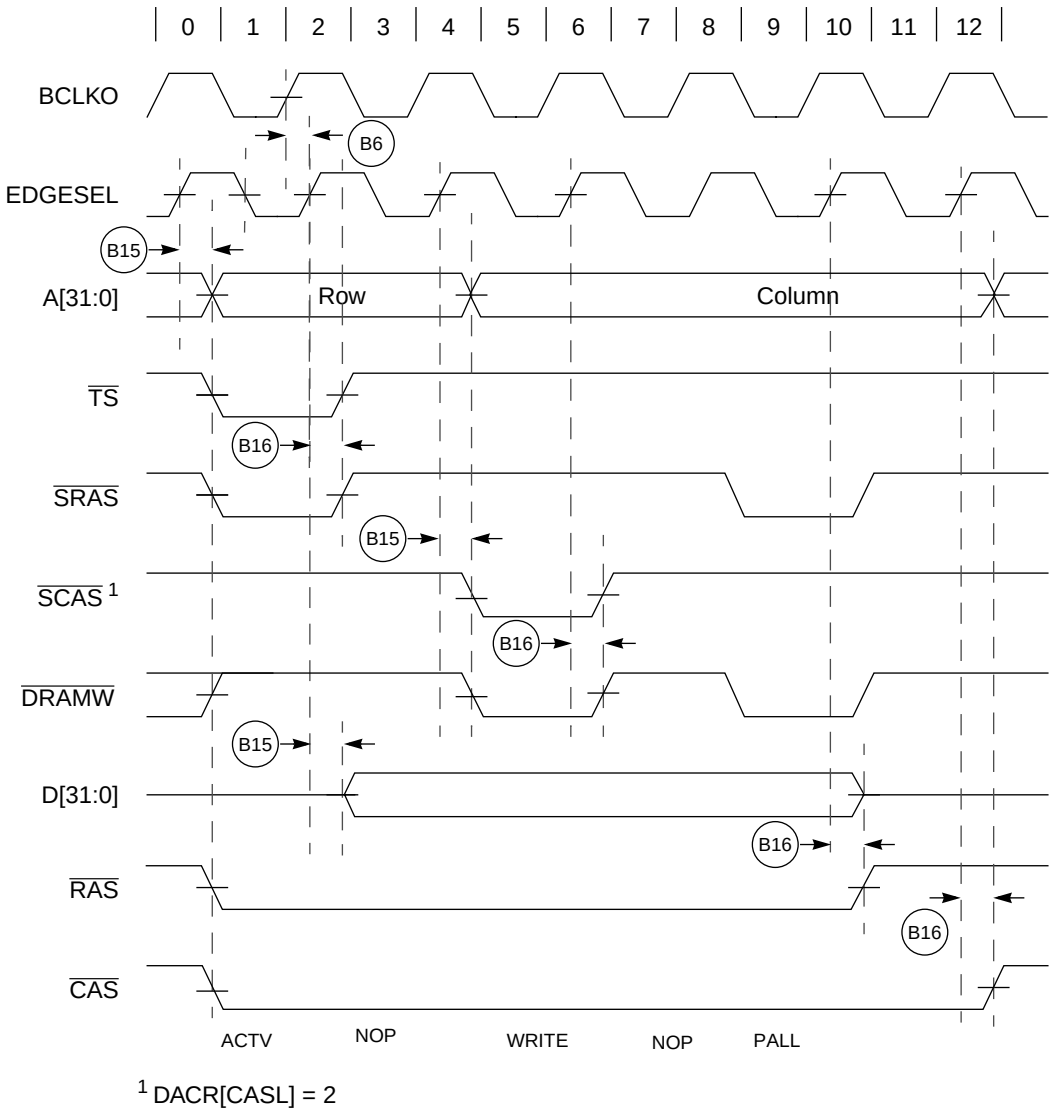


Figure 20-5. SDRAM Write Cycle with EDGESEL Tied to Buffered BCLKO

Figure 20-6 shows an SDRAM read cycle with EDGESEL tied high.

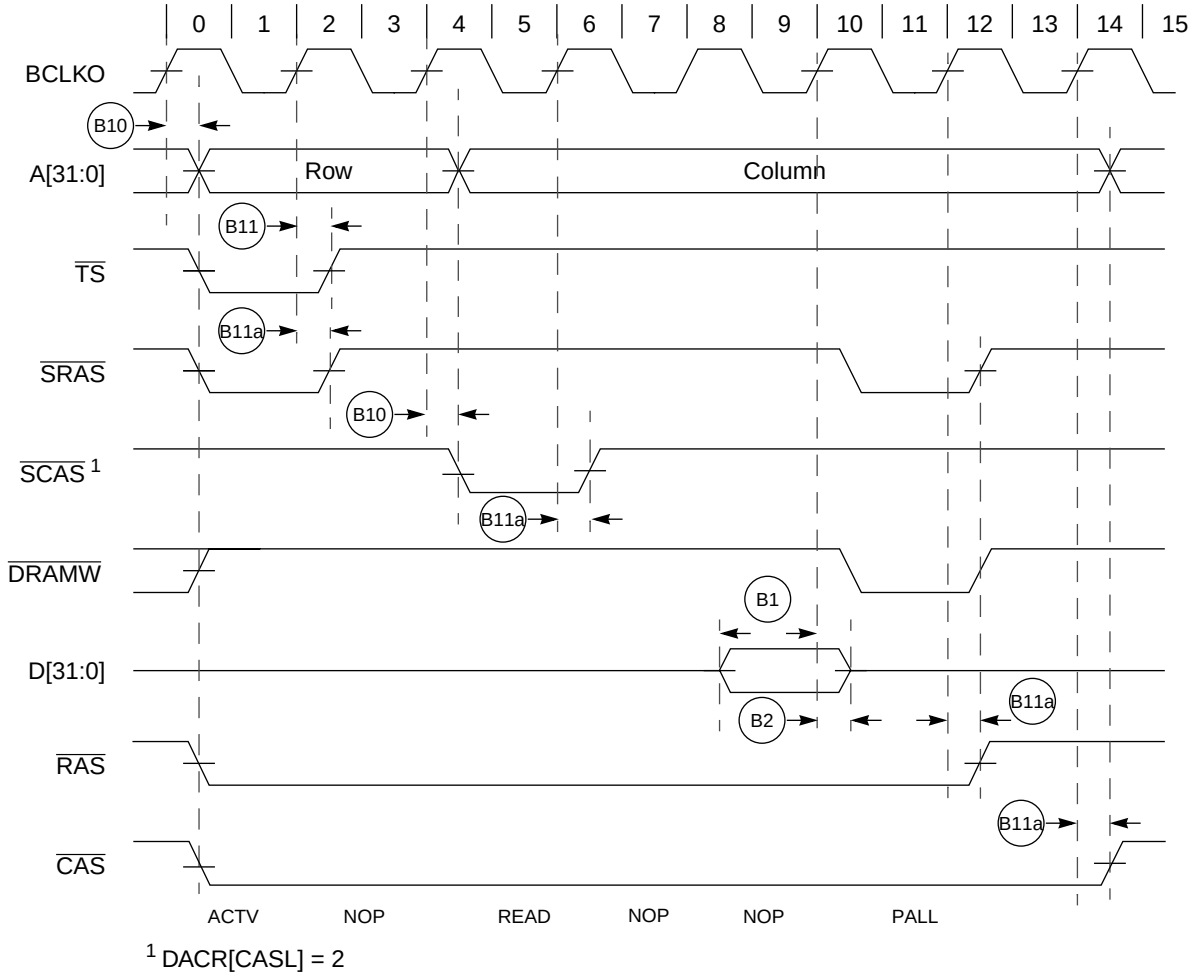


Figure 20-6. SDRAM Read Cycle with EDGESEL Tied High

Figure 20-7 shows an SDRAM write cycle with EDGESEL tied high.

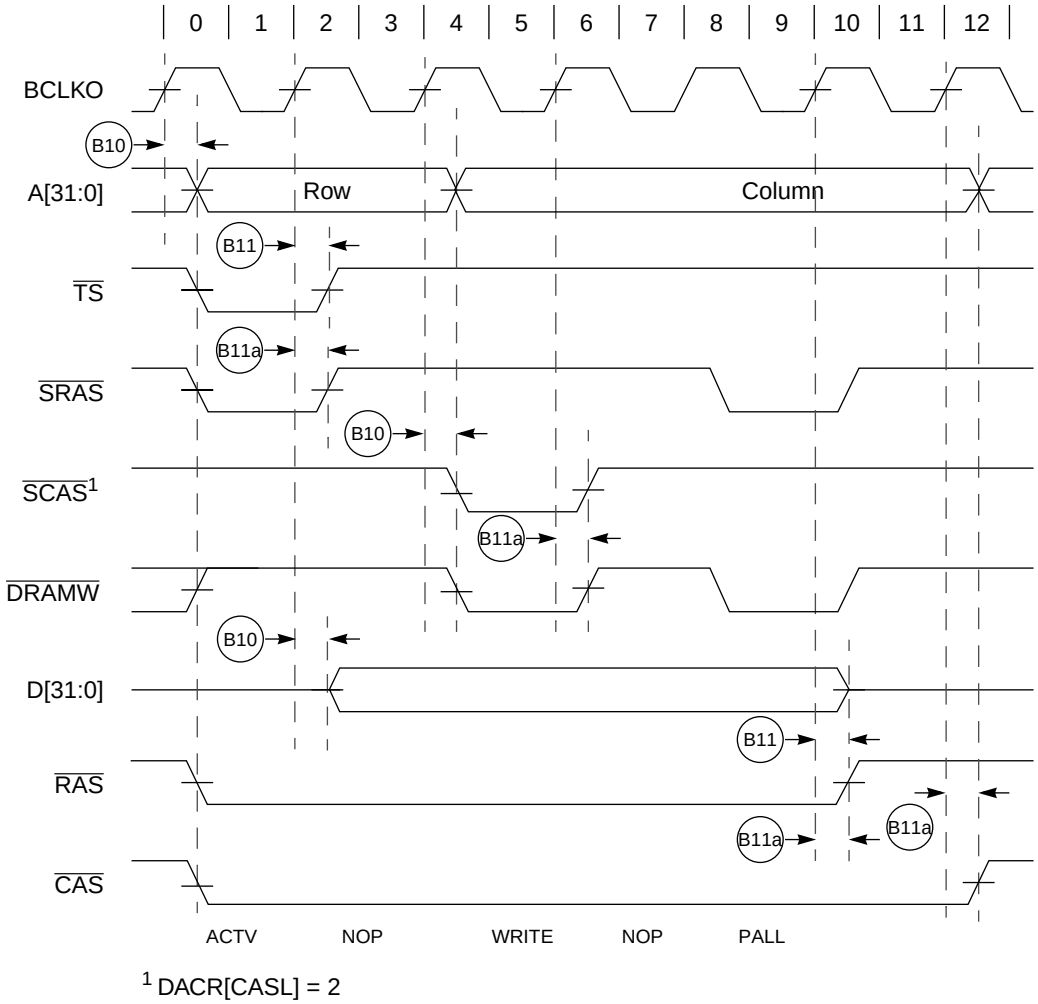
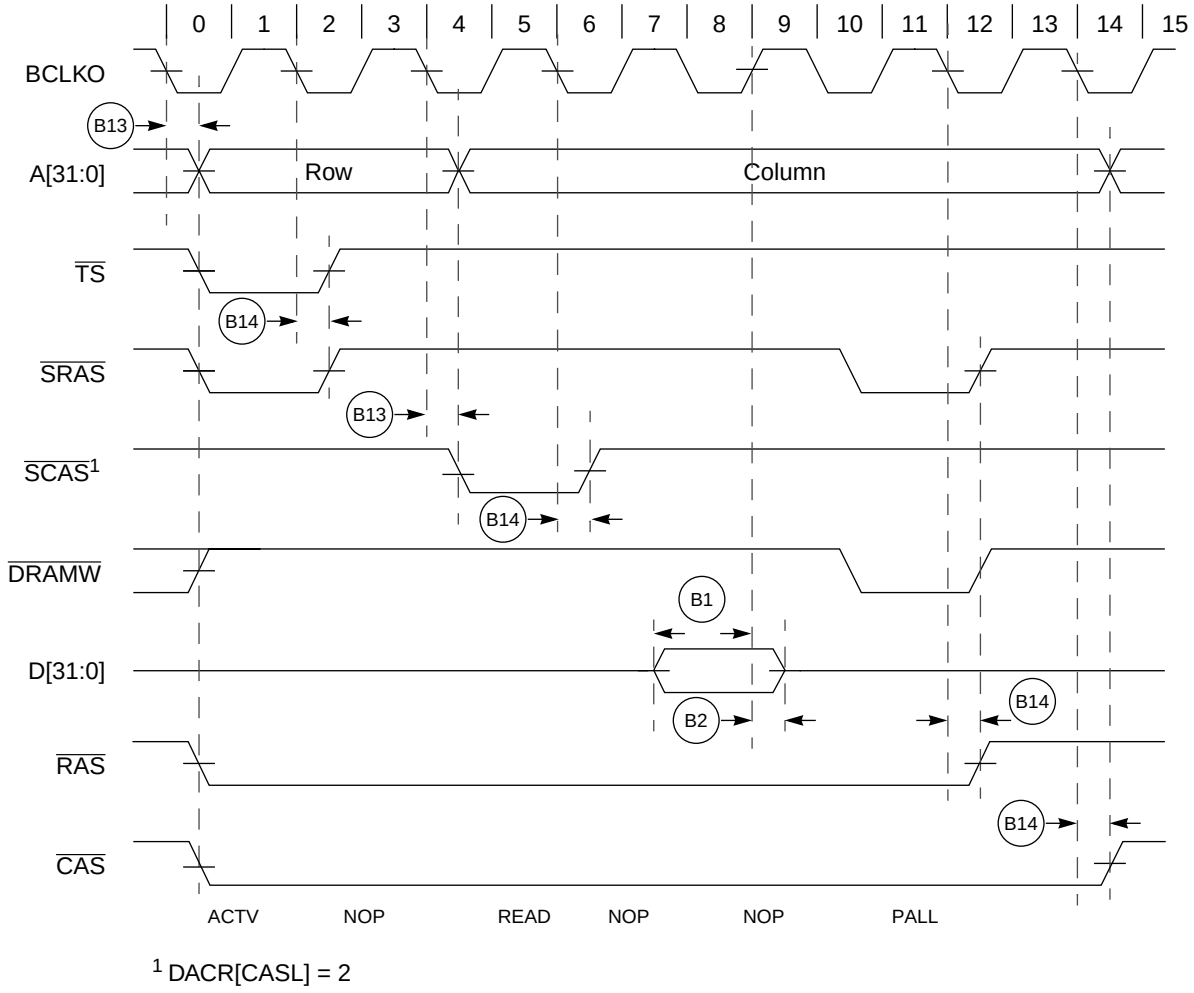


Figure 20-7. SDRAM Write Cycle with EDGESEL Tied High

Figure 20-8 shows an SDRAM read cycle with EDGESEL tied low.



[1] DACR[CASL] = 2

Figure 20-8. SDRAM Read Cycle with EDGESEL Tied Low

Figure 20-9 shows an SDRAM write cycle with EDGESEL tied low.

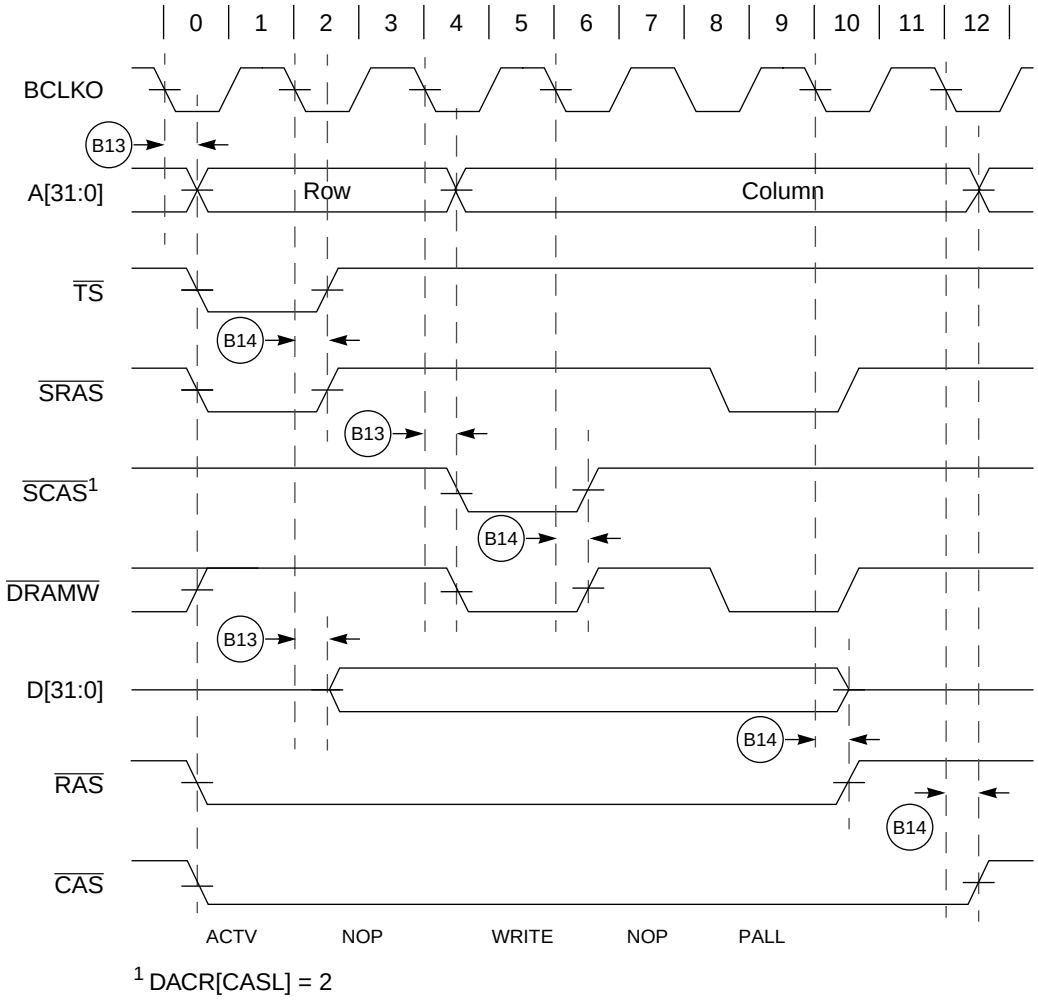


Figure 20-9. SDRAM Write Cycle with EDGESEL Tied Low

Figure 20-10 shows AC timing showing high impedance.

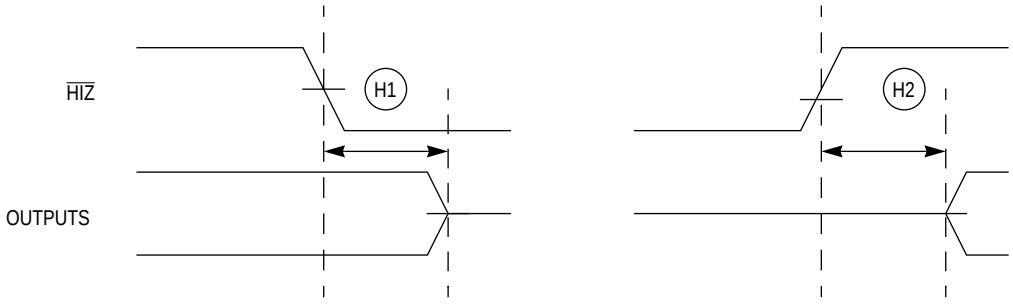


Figure 20-10. AC Output Timing—High Impedance

20.4 Reset Timing Specifications

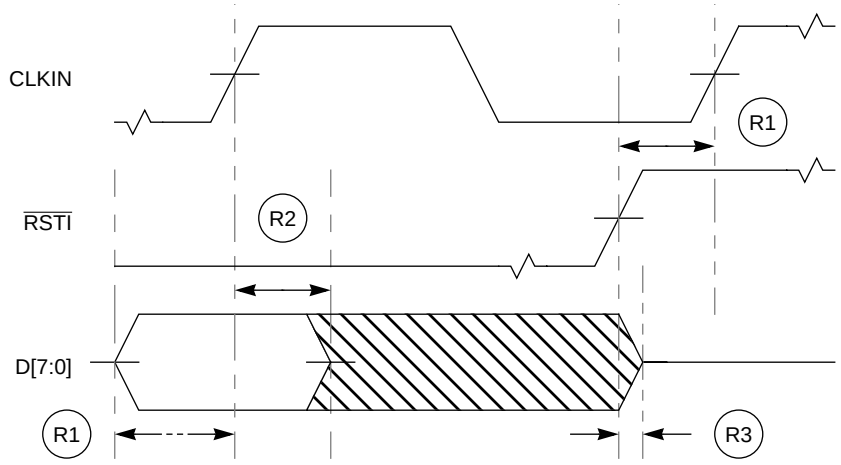
Table 20-7 lists specifications for the reset timing parameters shown in Figure 20-11.

Table 20-7. Reset Timing Specification

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
R1 [1]	Valid to CLKIN (setup)	7.5	—	5.5	—	nS
R2	CLKIN to invalid (hold)	3	—	2	—	nS
R3	$\overline{\text{RSTI}}$ to invalid (hold)	3	—	2	—	nS

[1] $\overline{\text{RSTI}}$ and D[7:0] are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

Figure 20-11 shows reset timing for the values in Table 20-7.



Note: Mode selects are registered on the rising CLKIN edge before the cycle in which $\overline{\text{RSTI}}$ is recognized as being negated.

Figure 20-11. Reset Timing

20.5 Debug AC Timing Specifications

Table 20-8 lists specifications for the debug AC timing parameters shown in Figure 20-13.

Table 20-8. Debug AC Timing Specification

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
D1	PST, DDATA to PSTCLK setup	7.5		5.5		nS
D2	PSTCLK to PST, DDATA hold	7.5		5.5		nS
D3	DSI-to-DSCLK setup	1		1		PSTCLKs

Table 20-8. Debug AC Timing Specification

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
D4 [1]	DSCLK-to-DSO hold	4		4		PSTCLKs
D5	DSCLK cycle time	5		5		PSTCLKs

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

Figure 20-12 shows real-time trace timing for the values in Table 20-8.

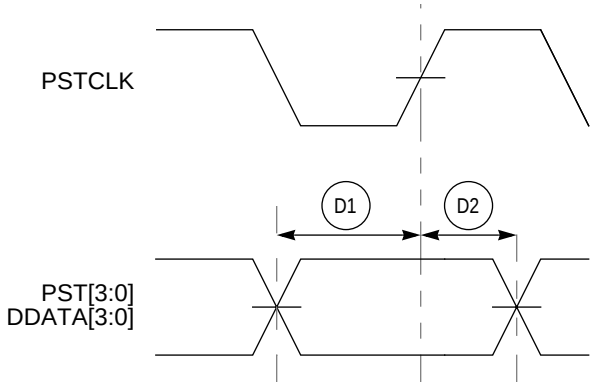


Figure 20-12. Real-Time Trace AC Timing

Figure 20-13 shows BDM serial port AC timing for the values in Table 20-8.

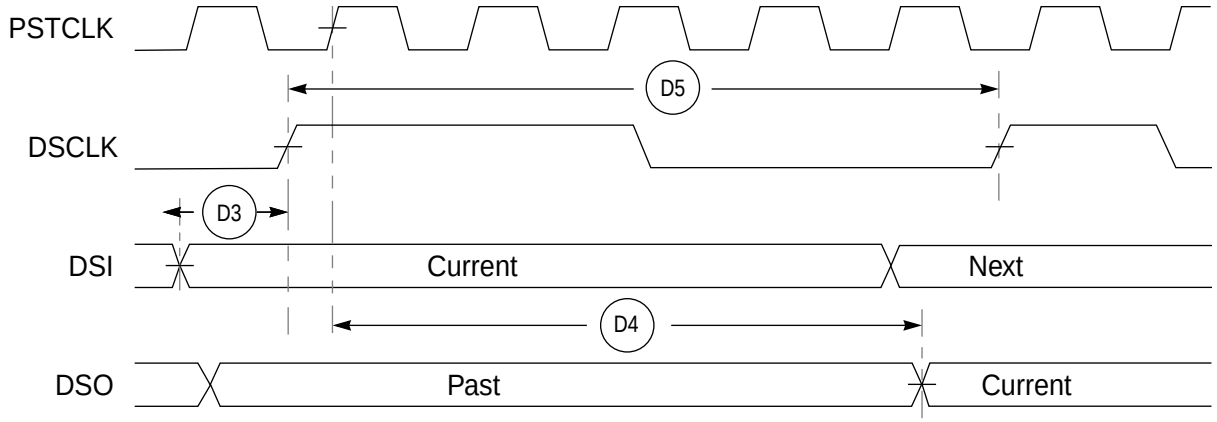


Figure 20-13. BDM Serial Port AC Timing

20.6 Timer Module AC Timing Specifications

Table 20-9 lists specifications for timer module AC timing parameters shown in Figure 20-14.

Figure 20-14 shows timings for Table 20-9.

Table 20-9. Timer Module AC Timing Specification

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
T1	TIN cycle time	3	—	3	—	Bus clocks
T2	TIN valid to BCLKO (input setup)	7.5	—	5.5	—	nS
T3	BCLKO to TIN invalid (input hold)	3	—	2	—	nS
T4	BCLKO to TOUT valid (output valid)	—	15	—	11	nS
T5	BCLKO to TOUT invalid (output hold)	1.5	—	1.5	—	nS
T6	TIN pulse width	1	—	1	—	Bus clocks
T7	TOUT pulse width	1	—	1	—	Bus clocks

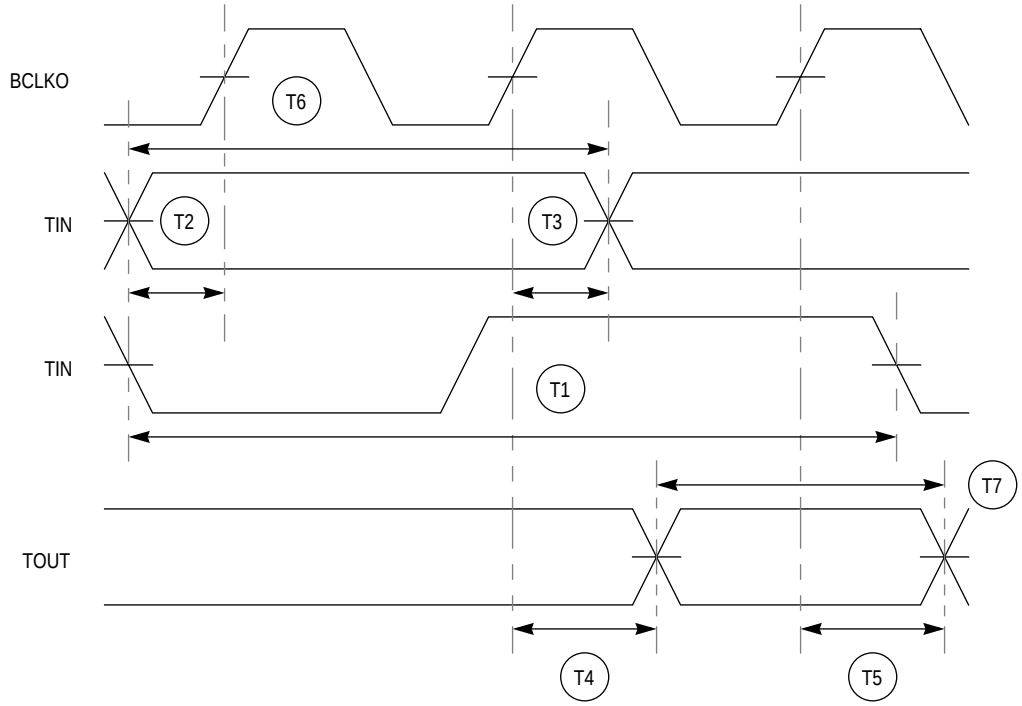


Figure 20-14. Timer Module AC Timing

20.7 I²C Input/Output Timing Specifications

Table 20-10 lists specifications for the I²C input timing parameters shown in Figure 20.8.

Table 20-10. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
I1	Start condition hold time	2	—	2	—	Bus clocks
I2	Clock low period	8	—	8	—	Bus clocks
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	—	1	mS
I4	Data hold time	0	—	0	—	nS
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	—	1	mS
I6	Clock high time	4	—	4	—	Bus clocks
I7	Data setup time	0	—	0	—	nS
I8	Start condition setup time (for repeated start condition only)	2	—	2	—	Bus clocks
I9	Stop condition setup time	2	—	2	—	Bus clocks

Table 20-11 lists specifications for the I²C output timing parameters shown in Figure 20.8.

Table 20-11. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
I1[1]	Start condition hold time	6	—	6	—	Bus clocks
I2 [1]	Clock low period	10	—	10	—	Bus clocks
I3 [2]	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	—	—	µS
I4 [1]	Data hold time	7	—	7	—	Bus clocks
I5 [3]	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	—	3	nS
I6 [1]	Clock high time	10	—	10	—	Bus clocks
I7 [1]	Data setup time	2	—	2	—	Bus clocks
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	20	—	Bus clocks
I9 [1]	Stop condition setup time	10	—	10	—	Bus clocks

1 Note: Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 20-11. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 20-11 are minimum values.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 20.8 shows timing for the values in Table 20-10 and Table 20-11.

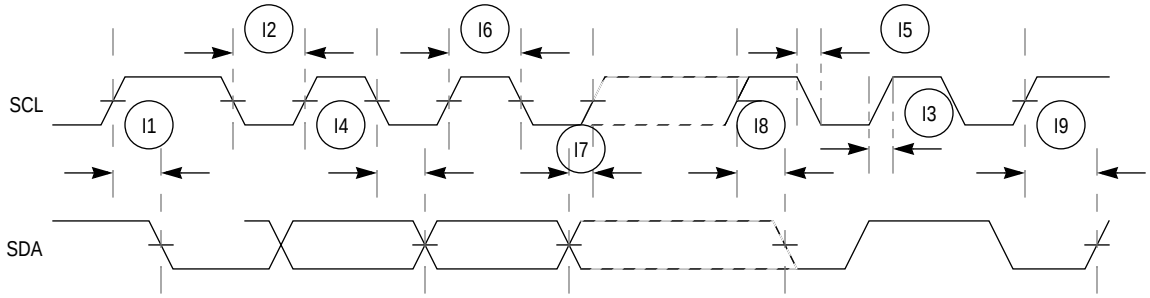


Figure 20-15. I^2C Input/Output Timings

20.8 UART Module AC Timing Specifications

Table 20-12 lists specifications for UART module AC timing parameters in Figure 20-16.

Table 20-12. UART Module AC Timing Specifications

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
U1	RXD valid to BCLKO (input setup)	7.5	—	5.5	—	nS
U2	BCLKO to RXD invalid (input hold)	3	—	2	—	nS
U3	$\overline{CTS}$ valid to BCLKO (input setup)	7.5	—	5.5	—	nS
U4	BCLKO to $\overline{CTS}$ invalid (input hold)	3	—	2	—	nS
U5	BCLKO to TXD valid (output valid)	—	15	—	11	nS
U6	BCLKO to TXD invalid (output hold)	1.5	—	1.5	—	nS
U7	BCLKO to $\overline{RTS}$ valid (output valid)	—	15	—	11	nS
U8	BCLKO to $\overline{RTS}$ invalid (output hold)	1.5	—	1.5	—	nS

Figure 20-16 shows UART timing for the values in Table 20-12.

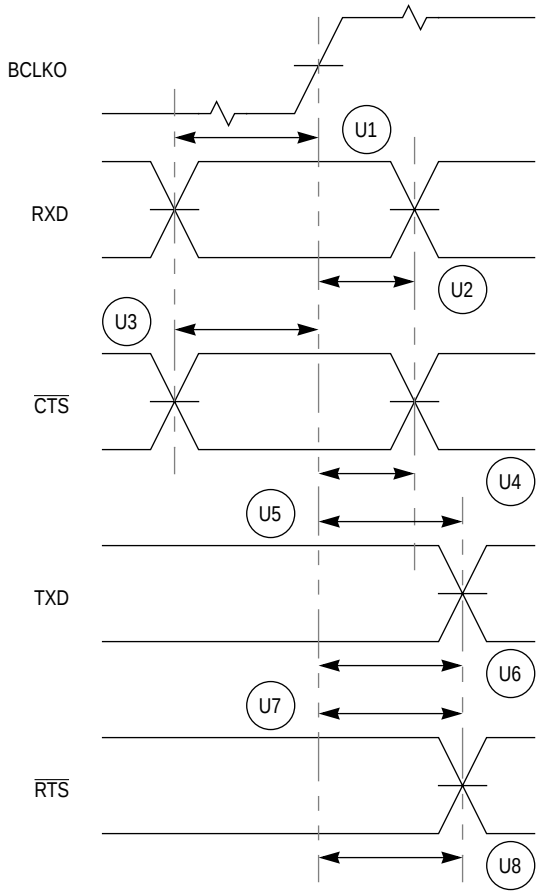


Figure 20-16. UART0/1 Module AC Timing—UART Mode

20.9 Parallel Port (General-Purpose I/O) Timing Specifications

Table 20-13 lists specifications for general-purpose I/O timing parameters in Figure 20-17.

Table 20-13. General-Purpose I/O Port AC Timing Specifications

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
P1	PP valid to BCLKO (input setup)	7.5	—	5.5	—	nS
P2	BCLKO to PP invalid (input hold)	3	—	2	—	nS
P3	BCLKO to PP valid (output valid)	—	15	—	11	nS
P4	BCLKO to PP invalid (output hold)	1	—	1	—	nS

Figure 20-17 shows general-purpose I/O timing.

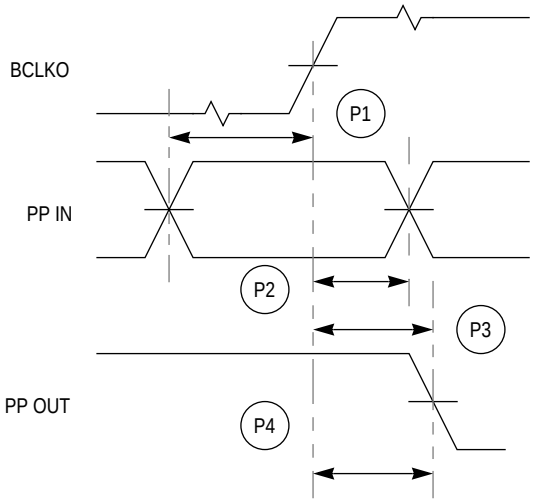


Figure 20-17. General-Purpose I/O Timing

20.10 DMA Timing Specifications

Table 20-14 lists specifications for DMA timing parameters shown in Figure 20-17.

Table 20-14. DMA AC Timing Specifications

Num	Characteristic	66 MHz		90 MHz		Units
		Min	Max	Min	Max	
M1	DREQ valid to BCLKO (input setup)	7.5	—	5.5	—	nS
M2	BCLKO to DREQ invalid (input hold)	3	—	2	—	nS

Figure 20-18 shows DMA AC timing.

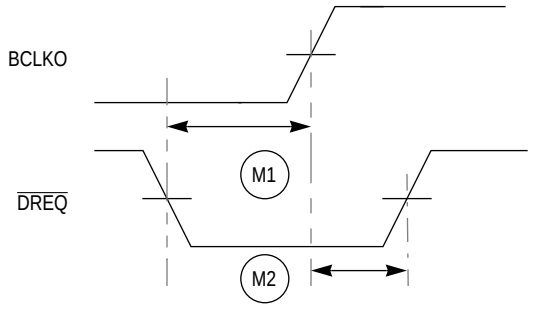


Figure 20-18. DMA Timing

20.11 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 20-15 lists specifications for JTAG AC timing parameters shown in Figure 20-19.

Table 20-15. IEEE 1149.1 (JTAG) AC Timing Specifications

Num	Characteristic	All Frequencies		Units
		Min	Max	
—	TCK frequency of operation	0	10	MHz
J1	TCK cycle time	100	—	nS
J2a	TCK clock pulse high width (measured at 1.5 V)	40	—	nS
J2b	TCK clock pulse low width (measured at 1.5 V)	40	—	nS
J3a	TCK fall time (V_{IH} = 2.4 V to V_{IL} = 0.5V)	—	5	nS
J3b	TCK rise time (V_{IL} = 0.5v to V_{IH} = 2.4V)	—	5	nS
J4	TDI, TMS to TCK rising (input setup)	10	—	nS
J5	TCK rising to TDI, TMS invalid (hold)	15	—	nS
J6	Boundary scan data valid to TCK (setup)	10	—	nS
J7	TCK to boundary-scan data invalid (hold)	15	—	nS
J8	$\overline{\text{TRST}}$ pulse width (asynchronous to clock edges)	15	—	—
J9	TCK falling to TDO valid (signal from driven or three-state)	—	30	nS
J10	TCK falling to TDO high impedance	—	30	nS
J11	TCK falling to boundary scan data valid (signal from driven or three-state)	—	30	nS
J12	TCK falling to boundary scan data high impedance	—	30	nS

Figure 20-19 shows JTAG timing.

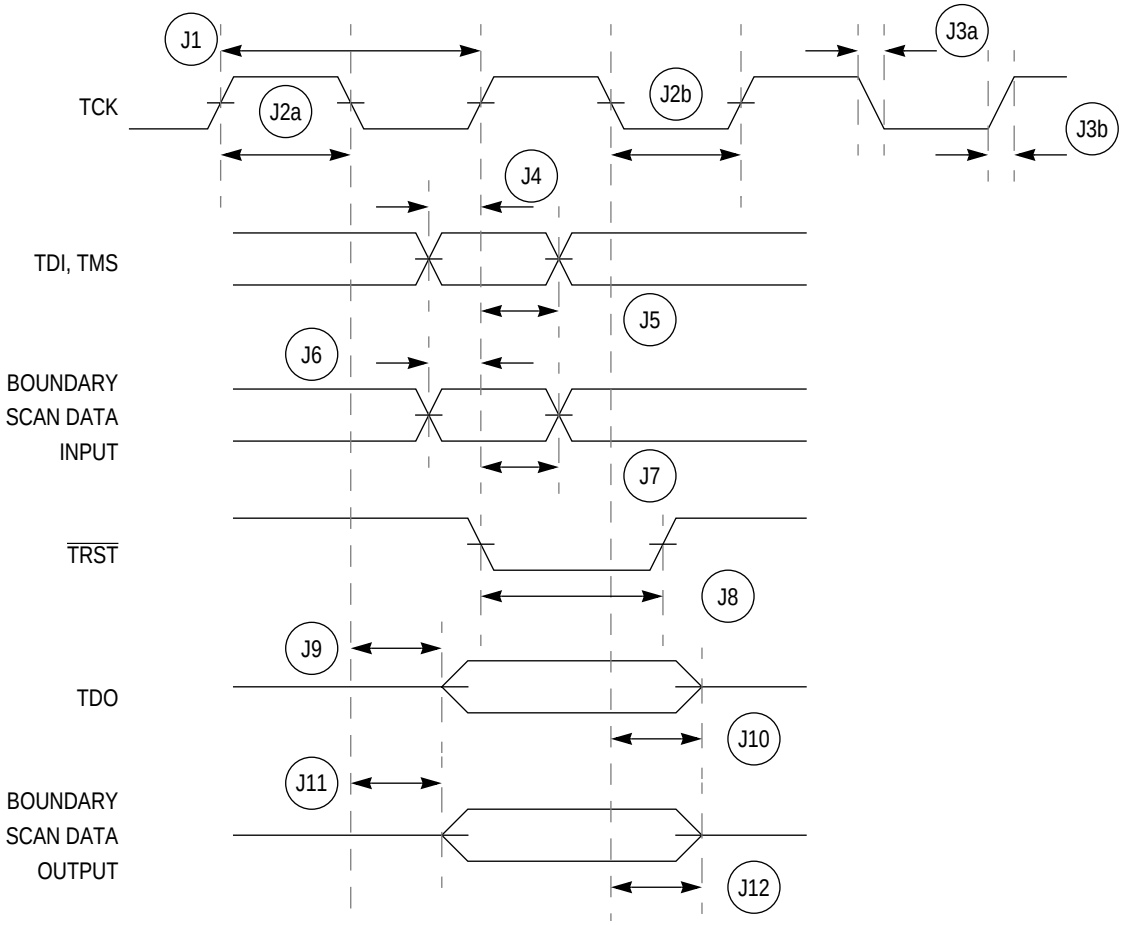


Figure 20-19. IEEE 1149.1 (JTAG) AC Timing