Chapter 9
Interrupt Controller

This chapter describes the operation of the interrupt controller portion of the system integration module (SIM). It includes descriptions of the registers in the interrupt controller memory map and the interrupt priority scheme.

9.1 Overview

The SIM provides a centralized interrupt controller for all MCF5307 interrupt sources, which consist of the following:

- External interrupts
- Software watchdog timer
- Timer modules
- I^2C module
- UART modules
- DMA module

Figure 9-1 is a block diagram of the interrupt controller.

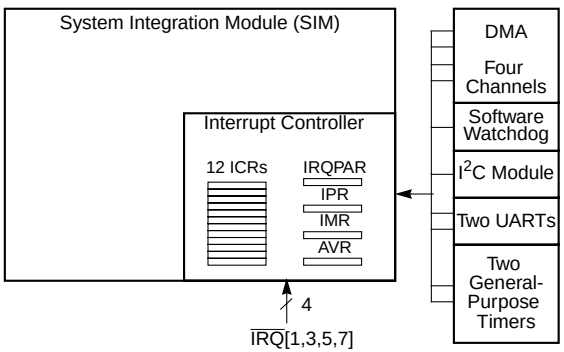

Figure 9-1. Interrupt Controller Block Diagram

The SIM provides the following registers for managing interrupts:

- Each potential interrupt source is assigned one of the 10 interrupt control registers (ICR0–ICR9), which are used to prioritize the interrupt sources.
- The interrupt mask register (IMR) provides bits for masking individual interrupt sources.
- The interrupt pending register (IPR) provides bits for indicating when an interrupt request is being made (regardless of whether it is masked in the IMR).
- The autovector register (AVEC) controls whether the SIM supplies an autovector or executes an external interrupt acknowledge cycle for each IRQ.
- The interrupt port assignment register (IRQPAR) provides the level assignment of the primary external interrupt pins—IRQ5, IRQ3, and IRQ1.

9.2 Interrupt Controller Registers

The interrupt controller register portion of the SIM memory map is shown in Table 9-2.

Table 9-1. Interrupt Controller Registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x040	Interrupt pending register (IPR) [p. 9-6]			
0x044	Interrupt mask register (IMR) [p. 9-6]			
0x048	Reserved			Autovector register (AVR) [p. 9-5]
Interrupt Control Registers (ICRs) [p. 9-3]				
0x04C	Software watchdog timer (ICR0) [p. 9-3]	Timer0 (ICR1) [p. 9-3]	Timer1 (ICR2) [p. 9-3]	I^2C (ICR3) [p. 9-3]
0x050	UART0 (ICR4) [p. 9-3]	UART1 (ICR5) [p. 9-3]	DMA0 (ICR6) [p. 9-3]	DMA1 (ICR7) [p. 9-3]
0x054	DMA2 (ICR8) [p. 9-3]	DMA3 (ICR9) [p. 9-3]	Reserved	

Each internal interrupt source has its own interrupt control register (ICR0–ICR9), shown in Table 9-2 and described in Section 9.2.1, “Interrupt Control Registers (ICR0–ICR9).”

Table 9-2. Interrupt Control Registers

MBAR Offset	Register	Name
0x04C	ICR0	Software watchdog timer
0x04D	ICR1	Timer0
0x04E	ICR2	Timer1
0x04F	ICR3	I^2C
0x050	ICR4	UART0
0x051	ICR5	UART1
0x052	ICR6	DMA0

Table 9-2. Interrupt Control Registers (Continued)

MBAR Offset	Register	Name
0x053	ICR7	DMA1
0x054	ICR8	DMA2
0x055	ICR9	DMA3

Internal interrupts are programmed to a level and priority. Each internal interrupt has a unique ICR. Each of the 7 interrupt levels has 5 priorities, for a total of 35 possible priority levels, encompassing internal and external interrupts. The four external interrupt pins offer seven possible settings at a fixed interrupt level and priority.

The IRQPAR determines these settings for external interrupt request levels. External interrupts can be programmed to supply an autovector or execute an external interrupt acknowledge cycle. This is described in Section 9.2.2, “Autovector Register (AVR).”

9.2.1 Interrupt Control Registers (ICR0–ICR9)

The interrupt control registers (ICR0–ICR9) provide bits for defining the interrupt level and priority for the interrupt source assigned to the ICR, shown in Table 9-2.

	7	6	5	4	3	2	1	0
Field	AVEC	—		IL			IP	
Reset	0	—		0_00			00	
R/W	R/W							
Address	MBAR + 0x04C (ICR0); 0x04D (ICR1); 0x04E (ICR2); 0x04F (ICR3); 0x050 (ICR4); 0x051 (ICR5); 0x052 (ICR6); 0x053 (ICR7); 0x054 (ICR8); 0x055 (ICR9)							

Figure 9-2. Interrupt Control Registers (ICR0–ICR9)

Table 9-3 describes ICR fields.

Table 9-3. ICR*n* Field Descriptions

Bits	Field	Description
7	AVEC	Autovector enable. Determines whether the interrupt-acknowledge cycle input (for the internal interrupt level indicated in IL for each interrupt) requires an autovector response. 0 Interrupting source returns vector during interrupt-acknowledge cycle. 1 SIM generates autovector during interrupt acknowledge cycle.
6–5	—	Reserved, should be cleared.
4–2	IL	Interrupt level. Indicates the interrupt level assigned to each interrupt input. See Table 9-4.
1–0	IP	Interrupt priority. Indicates the interrupt priority for internal modules within the interrupt-level assignment. See Table 9-4. 00 Lowest 01 Low 10 High 11 Highest

NOTE:

Assigning the same interrupt level and priority to multiple ICRs causes unpredictable system behavior.

Table 9-4 shows possible priority schemes for internal and external sources of the MCF5307. The internal module interrupt source in this table can be any internal interrupt source programmed to the given level and priority.

This table shows how external interrupts are prioritized with respect to internal interrupt sources within the same level. For example, UART0 and UART1 sources are programmed to IL = 110; in this case, UART0 is given lower priority than UART1, so ICR4[IP] = 01 and the ICR5[IP] = 10. $\overline{\text{IRQ3}}$ is programmed to level 6. If all three assert an interrupt request at the same time, they are serviced in the following order:

1. ICR5[IL] = 110 and ICR5[IP] = 10, so UART1 is serviced first (priority 7 in Table 9-4).
2. External interrupt IRQ3, set to level 6, is serviced next (priority 8).
3. ICR4[IL] = 110 and ICR5[IP] = 01, so UART0 is serviced last (priority 9).

Table 9-4. Interrupt Priority Scheme

Priority	Interrupt Level	ICR		Interrupt Source	IRQPAR[IRQPAR]
		IL	IP		
1	7	111	11	Internal module	xxx
2		111	10		xxx
3		xxx	xx	External interrupt pin IRQ7	xxx
4		111	01	Internal module	xxx
5		111	00		xxx
6	6	110	11	Internal module	xxx
7		110	10		xxx
8		xxx	xx	External interrupt pin IRQ3 (programmed as IRQ6)	x1x
9		110	01	Internal module	xxx
10		110	00		xxx
11	5	101	11	Internal module	xxx
12		101	10		xxx
13		xxx	xx	External interrupt pin IRQ5	0xx
14		101	01	Internal module	xxx
15		101	00		xxx

Table 9-4. Interrupt Priority Scheme (Continued)

Priority	Interrupt Level	ICR		Interrupt Source	IRQPAR[IRQPAR]
		IL	IP		
16	4	100	11	Internal module	xxx
17		100	10		xxx
18		xxx	xx	External interrupt pin IRQ5 (programmed as IRQ4)	1xx
19		100	01	Internal module	xxx
20		100	00		xxx
21	3	011	11	Internal module	xxx
22		011	10		xxx
23		xxx	xx	External interrupt pin IRQ3	x0x
24		011	01	Internal module	xxx
25		011	00		xxx
26	2	010	11	Internal module	xxx
27		010	10		xxx
28		xxx	xx	External interrupt pin IRQ1 (programmed as IRQ2)	xx1
29		010	01	Internal module	xxx
30		010	00		xxx
31	1	001	11	Internal module	xxx
32		001	10		xxx
33		xxx	xx	External interrupt pin IRQ1	xx0
34		001	01	Internal module	xxx
35		001	00		xxx

9.2.2 Autovector Register (AVR)

The autovector register (AVR), shown in Figure 9-3, enables external interrupt sources to be autovectored, using the vector offset defined in Table 2-19 in Section 2.8, “Exception Processing Overview.” Note that the autovector enable for internal interrupt sources applies for respective ICRs.

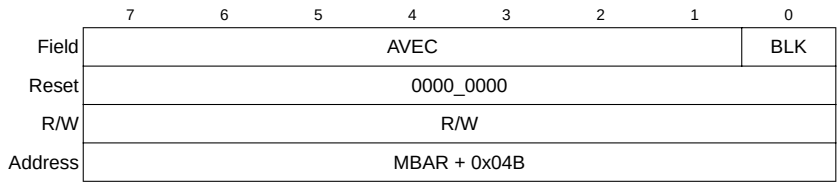

Figure 9-3. Autovector Register (AVR)

Table 9-5 describes AVR fields.

Table 9-5. AVR Field Descriptions

Bit	Name	Description
7–1	AVEC	Autovector control. Determines whether the external interrupt at that level is autovectored. 0 Interrupting source returns vector during interrupt-acknowledge cycle. 1 SIM generates autovector during interrupt-acknowledge cycle.
0	BLK	Block address strobe ($\overline{AS}$) for external AVEC access. Available for users who use $\overline{AS}$ as a global chip select for peripherals and do not want to enable them during an AVEC cycle. 0 Do not block address strobe. 1 Block address strobe from asserting.

Table 9-6 shows the correlation between AVR[AVEC] and the external interrupts. Note that an AVEC*n* bit is valid only when the corresponding external interrupt request level is enabled in the IRQPAR.

Table 9-6. Autovector Register Bit Assignments

Autovector Interrupt Source	Autovector Register Bit Location	Vector Offset
External interrupt request 1	AVEC1	0x64
External interrupt request 2	AVEC2	0x68
External interrupt request 3	AVEC3	0x6C
External interrupt request 4	AVEC4	0x70
External interrupt request 5	AVEC5	0x74
External interrupt request 6	AVEC6	0x78
External interrupt request 7	AVEC7	0x7C

9.2.3 Interrupt Pending and Mask Registers (IPR and IMR)

The interrupt pending register (IPR), Figure 9-4, makes visible the interrupt sources that have an interrupt pending. The interrupt mask register (IMR), also shown in Figure 9-4, is used to mask the internal and external interrupt sources.

NOTE:

To mask interrupt sources, first set the core's status register interrupt mask level to that of the source being masked in the IMR. Then, the IMR bit can be masked.

An interrupt is masked by setting, and enabled by clearing, the corresponding IMR bit. When a masked interrupt occurs, the corresponding IPR bit is still set, but no interrupt request is passed to the core.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	—														DMA3	DMA2
Reset	—														1	1
R/W	Read-only (IPR); R/W (IMR)															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	DMA1	DMA0	UART1	UART0	I2C	TIMER2	TIMER1	SWT	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	—
Reset	1111				1111				1111				1	1	1	—
R/W	Read-only (IPR); R/W (IMR)															
Addr	MBAR + 0x040 (IPR); + 0x044 (IMR)															

Figure 9-4. Interrupt Pending Register (IPR) and Interrupt Mask Register (IMR)

Table 9-7 describes IPR and IMR fields.

Table 9-7. IPR and IMR Field Descriptions

Bits	Name	Description
31–18	—	Reserved, should be cleared.
17–1	See Figure 9-4	Interrupt pending/mask. Each bit corresponds to an interrupt source defined by the ICR. The corresponding IMR bit determines whether an interrupt condition can generate an interrupt. At every clock, the IPR samples the signal generated by the interrupting source. The corresponding IPR bit reflects the state of the interrupt signal even if the corresponding IMR bit is set. 0 The corresponding interrupt source is not masked (IMR) and has no interrupt pending (IPR). 1 The corresponding interrupt source is masked (IMR) and has an interrupt pending (IPR)

9.2.4 Interrupt Port Assignment Register (IRQPAR)

The interrupt port assignment register (IRQPAR), shown in Figure 9-5, provides the level assignment of the primary external interrupt pins—IRQ5, IRQ3, and IRQ1. The setting of IRQPAR2–IRQPAR0 determines the interrupt level of these external interrupt pins.

	7	6	5	4	3	2	1	0
Field	IRQPAR2	IRQPAR1	IRQPAR0	—				
Reset	0000_0000							
R/W	R/W							
Address	MBAR + 0x06							

Figure 9-5. Interrupt Port Assignment Register (IRQPAR)

Table 9-8 describes IRQPAR fields.

Table 9-8. IRQPAR Field Descriptions

Bits	Name	Description
7–5	IRQPARn	Configures the IRQ pin assignments and priorities IRQPARn — External Pin — IRQPARn = 0 — IRQPARn = 1 IRQPAR2 — IRQ5 — Level 5 — Level 4 IRQPAR1 — IRQ3 — Level 3 — Level 6 IRQPAR0 — IRQ1 — Level 1 — Level 2
4–0	—	Reserved, should be cleared.