Chapter 19
IEEE 1149.1 Test Access Port (JTAG)

This chapter describes configuration and operation of the MCF5307 JTAG test implementation. It describes the use of JTAG instructions and provides information on how to disable JTAG functionality.

19.1 Overview

The MCF5307 dedicated user-accessible test logic is fully compliant with the publication *Standard Test Access Port and Boundary-Scan Architecture,* IEEE Standard 1149.1. Use the following description in conjunction with the supporting IEEE document listed above. This section includes the description of those chip-specific items that the IEEE standard requires as well as those items specific to the MCF5307 implementation.

The MCF5307 JTAG test architecture supports circuit board test strategies based on the IEEE standard. This architecture provides access to all data and chip control pins from the board-edge connector through the standard four-pin test access port (TAP) and the JTAG reset pin, $\overline{\text{TRST}}$. Test logic design is static and is independent of the system logic except where the JTAG is subordinate to other complimentary test modes, as described in Chapter 5, “Debug Support.” When in subordinate mode, JTAG test logic is placed in reset and the TAP pins can be used for other purposes, as described in Table 19-1.

The MCF5307 JTAG implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Bypass the MCF5307 by reducing the shift register path to a single cell
- Set MCF5307 output drive pins to fixed logic values while reducing the shift register path to a single cell
- Sample MCF5307 system pins during operation and transparently shift out the result
- Protect MCF5307 system output and input pins from backdriving and random toggling (such as during in-circuit testing) by placing all system pins in high-impedance state

NOTE:

IEEE Standard 1149.1 may interfere with system designs that do not incorporate JTAG capability. Section 19.6, “Disabling IEEE Standard 1149.1 Operation,” describes precautions for ensuring that this logic does not affect system or debug operation.

Figure 19-1 is a block diagram of the MCF5307 implementation of the 1149.1 IEEE standard. The test logic includes several test data registers, an instruction register, instruction register control decode, and a 16-state dedicated TAP controller.

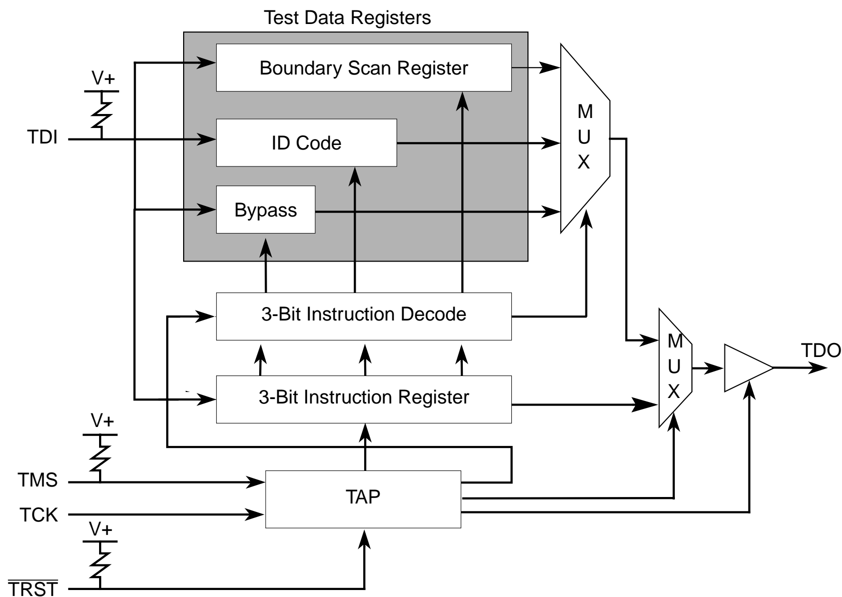


Figure 19-1. JTAG Test Logic Block Diagram

19.2 JTAG Signal Descriptions

JTAG operation on the MCF5307 is enabled when MTMOD0 is high (logic 1), as described in Table 19-1. Otherwise, JTAG TAP signals, TCK, TMS, TDI, TDO, and $\overline{\text{TRST}}$, are interpreted as the debug port pins. MTMOD0 should not be changed while $\overline{\text{RSTI}}$ is asserted.

Table 19-1. JTAG Pin Descriptions

Pin	Description
TCK	Test clock. The dedicated JTAG test logic clock is independent of the MCF5307 processor clock. Various JTAG operations occur on the rising or falling edge of TCK. Internal JTAG controller logic is designed such that holding TCK high or low indefinitely does cause the JTAG test logic to lose state information. If TCK is not used, it should be tied to ground.
TMS/ $\overline{\text{BKPT}}$	Test mode select (MTMOD0 high)/breakpoint (MTMOD0 low). TMS provides the JTAG controller with information to determine the test operation mode. The states of TMS and of the internal 16-state JTAG controller state machine at the rising edge of TCK determine whether the JTAG controller holds its current state or advances to the next state. This directly controls whether JTAG data or instruction operations occur. TMS has an internal pull-up, so if it is not driven low, its value defaults to a logic level of 1. If TMS is not used, it should be tied to VDD. $\overline{\text{BKPT}}$ signals a hardware breakpoint to the processor in debug mode. See Chapter 5, “Debug Support.”

Table 19-1. JTAG Pin Descriptions

Pin	Description
TDI/DSI	Test data input (MTMOD0 high)/development serial input (MTMOD0 low). TDI provides the serial data port for loading the JTAG boundary-scan, bypass, and instruction registers. Shifting in of data depends on the state of the JTAG controller state machine and the instruction in the instruction register. This shift occurs on the rising edge of TCK. TDI has an internal pull-up so if it is not driven low its value defaults to a logical 1. If TDI is not used, it should be tied to VDD. DSI provides single-bit communication for debug module commands. See Chapter 5, “Debug Support.”
TDO/ DSO	Test data output (MTMOD0 high)/development serial output (MTMOD0 low). TDO is the serial data port for outputting data from JTAG logic. Shifting data out depends on the state of the JTAG controller state machine and the instruction currently in the instruction register. This shift occurs on the falling edge of TCK. When not outputting test data, TDO is three-stated. It can also be placed in three-state mode to allow bussed or parallel connections to other devices having JTAG. DSO provides single-bit communication for debug module commands. See Chapter 5, “Debug Support.”
$\overline{\text{TRST}}$/ DSCLK	Test reset (MTMOD0 high)/development serial clock (MTMOD0 low). As $\overline{\text{TRST}}$, this pin asynchronously resets the internal JTAG controller to the test logic reset state, causing the JTAG instruction register to choose the IDCODE instruction. When this occurs, all JTAG logic is benign and does not interfere with normal MCF5307 functionality. Although this signal is asynchronous, Motorola recommends that $\overline{\text{TRST}}$ make only an asserted-to-negated transition while TMS is held at a logic 1 value. $\overline{\text{TRST}}$ has an internal pull-up; if it is not driven low its value defaults to a logic level of 1. However, if $\overline{\text{TRST}}$ is not used, it can either be tied to ground or, if TCK is clocked, to VDD. The former connection places the JTAG controller in the test logic reset state immediately; the latter connection eventually puts the JTAG controller (if TMS is a logic 1) into the test logic reset state after 5 TCK cycles. DSCLK is the development serial clock for the serial interface to the debug module.The maximum DSCLK frequency is 1/2 the BCLKO frequency. See Chapter 5, “Debug Support.”

19.3 TAP Controller

The state of TMS at the rising edge of TCK determines the current state of the TAP controller. The TAP controller can follow two basic two paths, one for executing JTAG instructions and the other for manipulating JTAG data based on JTAG instructions. The various states of the TAP controller are shown in Figure 19-2. For more detail on each state, see the IEEE Standard 1149.1 JTAG document. Note that regardless of the TAP controller state, test-logic-reset can be entered if TMS is held high for at least five rising edges of TCK. Figure 19-2 shows the JTAG TAP controller state machine.

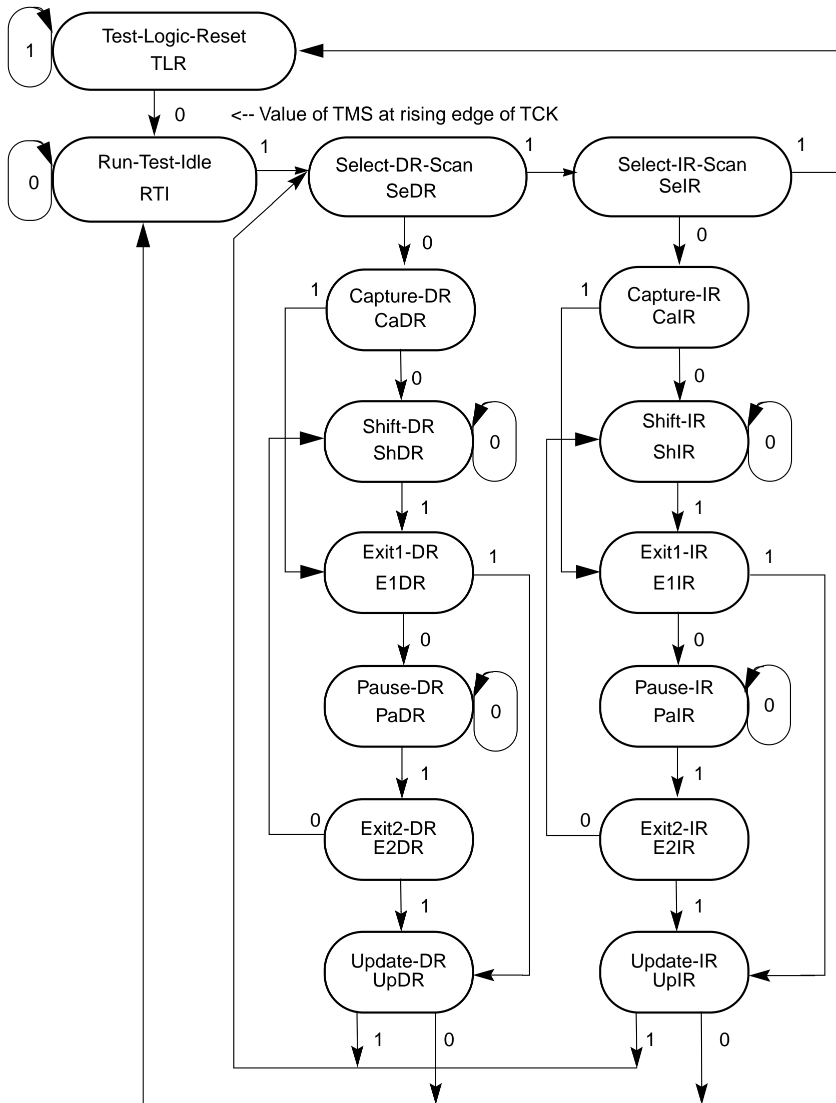


Figure 19-2. JTAG TAP Controller State Machine

19.4 JTAG Register Descriptions

The following sections describe the JTAG registers implemented on the MCF5307.

19.4.1 JTAG Instruction Shift Register

The MCF5307 IEEE Standard 1149.1 implementation uses a 3-bit instruction-shift register (IR) without parity. This register transfers its value to a parallel hold register and applies one of six instructions on the falling edge of TCK when the TAP state machine is in Update-IR state. To load instructions into the shift portion of the register, place the serial data on TDI before each rising edge of TCK. The msb of the instruction shift register is the bit closest to the TDI pin, and the lsb is the bit closest to TDO.

Table 19-2 describes customer-usable instructions.

Table 19-2. JTAG Instructions

Instruction	Class	IR	Description
EXTEST (EXT)	Required	000	Selects the boundary-scan register. Forces all output pins and bidirectional pins configured as outputs to the preloaded fixed values (with the SAMPLE/PRELOAD instruction) and held in the boundary-scan update registers. EXTEST can also configure the direction of bidirectional pins and establish high-impedance states on some pins. EXTEST becomes active on the falling edge of TCK in the Update-IR state when the data held in the instruction-shift register is equivalent to octal 0.
IDCODE (IDC)	Optional	001	Selects the IDCODE register for connection as a shift path between TDI and TDO. Interrogates the MCF5307 for version number and other part identification. The IDCODE register is implemented in accordance with IEEE Standard 1149.1 so the lsb of the shift register stage is set to logic 1 on the rising edge of TCK following entry into the capture-DR state. Therefore, the first bit shifted out after selecting the IDCODE register is always a logic 1. The remaining 31-bits are also set to fixed values. See Section 19.4.2, "IDCODE Register." IDCODE is the default value in the IR when a JTAG reset occurs by either asserting $\overline{\text{TRST}}$ or holding TMS high while clocking TCK through at least five rising edges and the falling edge after the fifth rising edge. A JTAG reset causes the TAP state machine to enter test-logic-reset state (normal operation of the TAP state machine into the test-logic-reset state also places the default value of octal 1 into the instruction register). The shift register portion of the instruction register is loaded with the default value of octal 1 in Capture-IR state and a TCK rising edge occurs.
SAMPLE/ PRELOAD (SMP)	Required	100	Provides two separate functions. It obtains a sample of the system data and control signals at the MCF5307 input pins and before the boundary-scan cell at the output pins. This sampling occurs on the rising edge of TCK in the capture-DR state when an instruction encoding of octal 4 is in the instruction register. Sampled data is observed by shifting it through the boundary-scan register to TDO by using shift-DR state. The data capture and shift are transparent to system operation. The users must provide external synchronization to achieve meaningful results because there is no internal synchronization between TCK and CLK. SAMPLE/PRELOAD also initializes the boundary-scan register update cells before selecting EXTEST or CLAMP. This is done by ignoring data shifted out of TDO while shifting in initialization data. The Update-DR state in conjunction with the falling edge of TCK can then transfer this data to the update cells. This data is applied to external outputs when an instruction listed above is applied.
HIGHZ (HIZ)	Optional	101	Anticipates the need to backdrive outputs and protects inputs from random toggling during board testing. Selects the bypass register, forcing all output and bidirectional pins into high-impedance. HIGHZ goes active on the falling edge of TCK in the Update-IR state when instruction shift register data held is equivalent to octal 5.

Table 19-2. JTAG Instructions (Continued)

Instruction	Class	IR	Description
CLAMP (CMP)	Optional	110	Selects the bypass register and asserts functional reset while forcing all output and bidirectional pins configured as outputs to fixed, preloaded values in the boundary-scan update registers. Enhances test efficiency by reducing the overall shift path to one bit (the bypass register) while conducting an EXTEST type of instruction through the boundary-scan register. CLAMP becomes active on the falling edge of TCK in the Update-IR state when instruction-shift register data is equivalent to octal 6.
BYPASS (BYP)	Required	111	Selects the single-bit bypass register, creating a single-bit shift register path from TDI to the bypass register to TDO. Enhances test efficiency by reducing the overall shift path when a device other than the MCF5307 is under test on a board design with multiple chips on the overall 1149.1 defined boundary-scan chain. The bypass register is implemented in accordance with 1149.1 so the shift register stage is set to logic 0 on the rising edge of TCK following entry into the capture-DR state. Therefore, the first bit shifted out after selecting the bypass register is always a logic 0 (to differentiate a part that supports an IDCODE register from a part that supports only the bypass register). BYPASS goes active on the falling edge of TCK in the Update-IR state when instruction shift register data is equivalent to octal 7.

The IEEE Standard 1149.1 requires the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. IDCODE, CLAMP, and HIGHZ are optional standard instructions that the MCF5307 implementation supports and are described in the IEEE Standard 1149.1.

19.4.2 IDCODE Register

The MCF5307 includes an IEEE Standard 1149.1-compliant JTAG identification register, IDCODE, which is read by the MCF5307 JTAG instruction encoded as octal 1.

31 30 29 28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Version Number (0000 forH55J, 0001 for J20C)	0	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1

Table 19-3 describes IDCODE bit assignments.

Table 19-3. IDCODE Bit Assignments

Bits	Description
31–28	Version number. Indicates the revision number of the MCF5307
27–22	Design center. Indicates the ColdFire design center
21–12	Device number. Indicates an MCF5307
11–1	Indicates the reduced JEDEC ID for Motorola. Joint Electron Device Engineering Council (JEDEC) Publication 106-A and Chapter 11 of the IEEE Standard 1149.1 give more information on this field.
0	Identifies this as the JTAG IDCODE register (and not the bypass register) according to the IEEE Standard 1149.1

19.4.3 JTAG Boundary-Scan Register

The MCF5307 model includes an IEEE Standard 1149.1-compliant boundary-scan register connected between TDI and TDO when the EXTEST or SAMPLE/PRELOAD instructions are selected. This register captures signal data on the input pins, forces fixed values on the output pins, and selects the direction and drive characteristics (a logic value or high impedance) of the bidirectional and three-state pins. Table 19-4 shows MCF5307 boundary-scan register bits.

Table 19-4. Boundary-Scan Bit Definitions

Bit	Cell Type	Pin Cell	Pin Type
0	O.Ctl	PP0 enable	—
1	O.Pin	PP0	I/O
2	I.Pin	PP0	I/O
3	IO.Ctl	PP1 enable	—
4	O.Pin	PP1	I/O
5	I.Pin	PP1	I/O
6	IO.Ctl	PP2 enable	—
7	O.Pin	PP2	I/O
8	I.Pin	PP2	I/O
9	IO.Ctl	PP3 enable	—
10	O.Pin	PP3	I/O
11	I.Pin	PP3	I/O
12	IO.Ctl	PP4 enable	—
13	O.Pin	PP4	I/O
14	I.Pin	PP4	I/O
15	IO.Ctl	PP5 enable	—
16	O.Pin	PP5	I/O
17	I.Pin	PP5	I/O
18	IO.Ctl	PP6 enable	—
19	O.Pin	PP6	I/O
20	I.Pin	PP6	I/O
21	IO.Ctl	PP7 enable	—
22	O.Pin	PP7	I/O
23	I.Pin	PP7	I/O
24	O.Pin	PST3	O
25	O.Pin	PST2	O
26	O.Pin	PST1	O
27	O.Pin	PST0	O
28	O.Pin	DDATA3	O
120	O.Pin	$\overline{\text{BE0}}$	O
121	O.Pin	SCKE	O
122	O.Pin	$\overline{\text{SCAS}}$	O
123	O.Pin	$\overline{\text{SRAS}}$	O
124	O.Pin	$\overline{\text{DRAMW}}$	O
125	O.Pin	$\overline{\text{CAS3}}$	O
126	O.Pin	$\overline{\text{CAS2}}$	O
127	O.Pin	$\overline{\text{CAS1}}$	O
128	O.Pin	$\overline{\text{CAS0}}$	O
129	O.Pin	$\overline{\text{RAS1}}$	O
130	O.Pin	$\overline{\text{RAS0}}$	O
131	I.Pin	TIN1	I
132	I.Pin	TIN0	I
133	O.Pin	TOUT0	O
134	O.Pin	TOUT1	O
135	I.Pin	$\overline{\text{BG}}$	I
136	O.Pin	$\overline{\text{BD}}$	O
137	O.Pin	$\overline{\text{BR}}$	O
138	I.Pin	$\overline{\text{IRQ1}}$	I
139	I.Pin	$\overline{\text{IRQ3}}$	I
140	I.Pin	$\overline{\text{IRQ5}}$	I
141	I.Pin	$\overline{\text{IRQ7}}$	I
142	I.Pin	$\overline{\text{RSTI}}$	I
143	O.Pin	$\overline{\text{TS}}$	I/O
144	I.Pin	$\overline{\text{TS}}$	I/O
145	IO.Ctl	$\overline{\text{TA}}$ enable	—
146	O.Pin	$\overline{\text{TA}}$	I/O
147	I.Pin	$\overline{\text{TA}}$	I/O
148	O.Pin	R/$\overline{\text{W}}$	I/O

Table 19-4. Boundary-Scan Bit Definitions

Bit	Cell Type	Pin Cell	Pin Type
29	O.Pin	DDATA2	O
30	O.Pin	DDATA1	O
31	O.Pin	DDATA0	O
32	O.Pin	PSTCLK	O
33	I.Pin	CLKIN	I
34	IO.Ctl	$\overline{\text{RSTO}}$ enable	—
35	O.Pin	$\overline{\text{RSTO}}$	I/O
36	I.Pin	$\overline{\text{RSTO}}$	I/O
37	O.Pin	BCLKO	O
38	I.Pin	EDGESEL	I
39	O.Pin	TXD0	O
40	I.Pin	RXD0	I
41	O.Pin	RTS0	O
42	I.Pin	CTS0	I
43	O.Pin	TXD1	O
44	I.Pin	RXD1	I
45	O.Pin	RTS1	O
46	I.Pin	CTS1	I
47	I.Pin	$\overline{\text{HIZ}}$	I
48	IO.Ctl	Data enable	—
49	O.Pin	D0	I/O
50	I.Pin	D0	I/O
51	O.Pin	D1	I/O
52	I.Pin	D1	I/O
53	O.Pin	D2	I/O
54	I.Pin	D2	I/O
55	O.Pin	D3	I/O
56	I.Pin	D3	I/O
57	O.Pin	D4	I/O
58	I.Pin	D4	I/O
59	O.Pin	D5	I/O
60	I.Pin	D5	I/O
61	O.Pin	D6	I/O
62	I.Pin	D6	I/O
63	O.Pin	D7	I/O
64	I.Pin	D7	I/O
149	I.Pin	R/$\overline{\text{W}}$	I/O
150	O.Pin	$\overline{\text{AS}}$	I/O
151	I.Pin	$\overline{\text{AS}}$	I/O
152	O.Pin	$\overline{\text{CS7}}$	O
153	O.Pin	$\overline{\text{CS6}}$	O
154	O.Pin	$\overline{\text{CS5}}$	O
155	O.Pin	$\overline{\text{CS4}}$	O
156	O.Pin	$\overline{\text{CS3}}$	O
157	O.Pin	$\overline{\text{CS2}}$	O
158	O.Pin	$\overline{\text{CS1}}$	O
159	O.Pin	$\overline{\text{CS0}}$	O
160	O.Pin	$\overline{\text{OE}}$	O
161	O.Pin	SIZ1	I/O
162	I.Pin	SIZ1	I/O
163	O.Pin	SIZ0	I/O
164	I.Pin	SIZ0	I/O
165	IO.Ctl	PP15 enable	—
166	I.Pin	PP15	I/O
167	O.Pin	PP15	I/O
168	IO.Ctl	PP14 enable	—
169	I.Pin	PP14	I/O
170	O.Pin	PP14	I/O
171	IO.Ctl	PP13 enable	—
172	I.Pin	PP13	I/O
173	O.Pin	PP13	I/O
174	IO.Ctl	PP12 enable	—
175	I.Pin	PP12	I/O
176	O.Pin	PP12	I/O
177	IO.Ctl	PP11 enable	—
178	I.Pin	PP11	I/O
179	O.Pin	PP11	I/O
180	IO.Ctl	PP10 enable	—
181	I.Pin	PP10	I/O
182	O.Pin	PP10	I/O
183	IO.Ctl	PP9 enable	—
184	I.Pin	PP9	I/O

Table 19-4. Boundary-Scan Bit Definitions

Bit	Cell Type	Pin Cell	Pin Type
65	O.Pin	D8	I/O
66	I.Pin	D8	I/O
67	O.Pin	D9	I/O
68	I.Pin	D9	I/O
69	O.Pin	D10	I/O
70	I.Pin	D10	I/O
71	O.Pin	D11	I/O
72	I.Pin	D11	I/O
73	O.Pin	D12	I/O
74	I.Pin	D12	I/O
75	O.Pin	D13	I/O
76	I.Pin	D13	I/O
77	O.Pin	D14	I/O
78	I.Pin	D14	I/O
79	O.Pin	D15	I/O
80	I.Pin	D15	I/O
81	O.Pin	D16	I/O
82	I.Pin	D16	I/O
83	O.Pin	D17	I/O
84	I.Pin	D17	I/O
85	O.Pin	D18	I/O
86	I.Pin	D18	I/O
87	O.Pin	D19	I/O
88	I.Pin	D19	I/O
89	O.Pin	D20	I/O
90	I.Pin	D20	I/O
91	O.Pin	D21	I/O
92	I.Pin	D21	I/O
93	O.Pin	D22	I/O
94	I.Pin	D22	I/O
95	O.Pin	D23	I/O
96	I.Pin	D23	I/O
97	O.Pin	D24	I/O
98	I.Pin	D24	I/O
99	O.Pin	D25	I/O
100	I.Pin	D25	I/O
185	O.Pin	PP9	I/O
186	IO.Ctl	PP8 enable	—
187	I.Pin	PP8	I/O
188	O.Pin	PP8	I/O
189	IO.Ctl	$\overline{TS}$/R/$\overline{W}$/SIZ enable	—
190	IO.Ctl	Address enable	—
191	O.Pin	A23	I/O
192	I.Pin	A23	I/O
193	O.Pin	A22	I/O
194	I.Pin	A22	I/O
195	O.Pin	A21	I/O
196	I.Pin	A21	I/O
197	O.Pin	A20	I/O
198	I.Pin	A20	I/O
199	O.Pin	A19	I/O
200	I.Pin	A19	I/O
201	O.Pin	A18	I/O
202	I.Pin	A18	I/O
203	O.Pin	A17	I/O
204	I.Pin	A17	I/O
205	O.Pin	A16	I/O
206	I.Pin	A16	I/O
207	O.Pin	A15	I/O
208	I.Pin	A15	I/O
209	O.Pin	A14	I/O
210	I.Pin	A14	I/O
211	O.Pin	A13	I/O
212	I.Pin	A13	I/O
213	O.Pin	A12	I/O
214	I.Pin	A12	I/O
215	O.Pin	A11	I/O
216	I.Pin	A11	I/O
217	O.Pin	A10	I/O
218	I.Pin	A10	I/O
219	O.Pin	A9	I/O
220	I.Pin	A9	I/O

Table 19-4. Boundary-Scan Bit Definitions

Bit	Cell Type	Pin Cell	Pin Type
101	O.Pin	D26	I/O
102	I.Pin	D26	I/O
103	O.Pin	D27	I/O
104	I.Pin	D27	I/O
105	O.Pin	D28	I/O
106	I.Pin	D28	I/O
107	O.Pin	D29	I/O
108	I.Pin	D29	I/O
109	O.Pin	D30	I/O
110	I.Pin	D30	I/O
111	O.Pin	D31	I/O
112	I.Pin	D31	I/O
113	O.Pin	SDA	OD
114	I.Pin	SDA	I
115	O.Pin	SCL	OD
116	I.Pin	SCL	I
117	O.Pin	$\overline{BE3}$	O
118	O.Pin	$\overline{BE2}$	O
119	O.Pin	$\overline{BE1}$	O
221	O.Pin	A8	I/O
222	I.Pin	A8	I/O
223	O.Pin	A7	I/O
224	I.Pin	A7	I/O
225	O.Pin	A6	I/O
226	I.Pin	A6	I/O
227	O.Pin	A5	I/O
228	I.Pin	A5	I/O
229	O.Pin	A4	I/O
230	I.Pin	A4	I/O
231	O.Pin	A3	I/O
232	I.Pin	A3	I/O
233	O.Pin	A2	I/O
234	I.Pin	A2	I/O
235	O.Pin	A1	I/O
236	I.Pin	A1	I/O
237	O.Pin	A0	I/O
238	I.Pin	A0	I/O

19.4.4 JTAG Bypass Register

The IEEE Standard 1149.1-compliant bypass register creates a single-bit shift register path from TDI to the bypass register to TDO when the BYPASS instruction is selected.

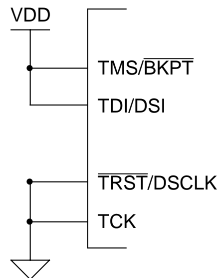
19.5 Restrictions

Test logic design is static, so TCK can be stopped in high or low state with no data loss. However, system logic uses a different system clock not internally synchronized to TCK. Operation mixing 1149.1 test logic with system functional logic that uses both clocks must coordinate and synchronize these clocks externally to the MCF5307.

19.6 Disabling IEEE Standard 1149.1 Operation

There are two ways to use the MCF5307 without IEEE Standard 1149.1 test logic being active:

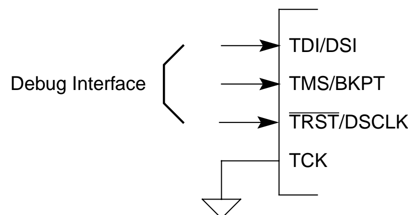
- Nonuse of JTAG test logic by either nontermination (disconnection) or intentionally fixing TAP logic values. The following issues must be addressed if IEEE Standard 1149.1 logic is not to be used when the MCF5307 is assembled onto a board.
  - IEEE Standard 1149.1 test logic must remain transparent and benign to the system logic during functional operation. To ensure that the part enters the test-logic-reset state requires either connecting $\overline{\text{TRST}}$ to logic 0 or connecting TCK to a source that supplies five rising edges and a falling edge after the fifth rising edge. The recommended solution is to connect $\overline{\text{TRST}}$ to logic 0.
  - TCK has no internal pull-up as is required on TMS, TDI, and $\overline{\text{TRST}}$; therefore, it must be terminated to preclude mid-level input values. Figure 19-4 shows pin values recommended for disabling JTAG with the MCF5307 in JTAG mode.



Note: MTMOD0 high allows JTAG mode.

Figure 19-4. Disabling JTAG in JTAG Mode

- Disabling JTAG test logic by holding MTMOD0 low during reset (debug mode). This allows the IEEE Standard 1149.1 test controller to enter test-logic-reset state when $\overline{\text{TRST}}$ is internally asserted to the controller. TAP pins function as debug mode pins. In JTAG mode, inputs TDI/DSI, TMS/$\overline{\text{BKPT}}$, and $\overline{\text{TRST}}$/DSCLK have internal pull-ups enabled. Figure 19-5 shows pin values recommended for disabling JTAG in debug mode.



Note: MTMOD0 low prohibits JTAG.

Figure 19-5. Disabling JTAG in Debug Mode

19.7 Obtaining the IEEE Standard 1149.1

The IEEE Standard 1149.1 JTAG specification is a copyrighted document and must be obtained directly from the IEEE:

IEEE Standards Department
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

http://stdsbbs.ieee.org/

FAX: 908-981-9667
Information: 908-981-0060 or 1-800-678-4333