Chapter 16
Mechanical Data

This chapter provides a function pin listing and package diagram for the MCF5307. See the website [http://www.motorola.com/coldfire] for any updated information.

16.1 Package

The MCF5307 is assembled in a 208-pin, thermally enhanced plastic QFP package.

16.2 Pinout

The MCF5307 pinout is detailed in the following tables, including the primary and secondary functions of multiplexed signals. Additional columns indicate the output drive capability of each pin, whether it is internally synchronized, and if the signal can change on a negative clock transition.

These tables show MCF5307 pin numbers, including signal multiplexing. Additional columns indicate the direction, description, and output drive capability of each pin.

Table 16-1. Pins 1–52 (Left, Top-to-Bottom)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
1	VCC	—	—	Power input	—
2	A0	—	I/O	Address bus bit	8
3	A1	—	I/O	Address bus bit	8
4	GND	—	—	Ground pin	—
5	A2	—	I/O	Address bus bit	8
6	A3	—	I/O	Address bus bit	8
7	VCC	—	—	Power input	—
8	A4	—	I/O	Address bus bit	8
9	A5	—	I/O	Address bus bit	8
10	GND	—	—	Ground pin	—
11	A6	—	I/O	Address bus bit	8
12	A7	—	I/O	Address bus bit	8

Table 16-1. Pins 1–52 (Left, Top-to-Bottom) (Continued)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
13	VCC	—	—	Power input	—
14	A8	—	I/O	Address bus bit	8
15	A9	—	I/O	Address bus bit	8
16	A10	—	I/O	Address bus bit	8
17	GND	—	—	Ground pin	—
18	A11	—	I/O	Address bus bit	8
19	A12	—	I/O	Address bus bit	8
20	A13	—	I/O	Address bus bit	8
21	VCC	—	—	Power input	—
22	A14	—	I/O	Address bus bit	8
23	A15	—	I/O	Address bus bit	8
24	A16	—	I/O	Address bus bit	8
25	GND	—	—	Ground pin	—
26	A17	—	I/O	Address bus bit	8
27	A18	—	I/O	Address bus bit	8
28	A19	—	I/O	Address bus bit	8
29	VCC	—	—	Power input	—
30	A20	—	I/O	Address bus bit	8
31	A21	—	I/O	Address bus bit	8
32	A22	—	I/O	Address bus bit	8
33	GND	—	—	Ground pin	—
34	A23	—	I/O	Address bus bit	8
35	PP8	A24	I/O	Parallel port bit/Address bus bit	8
36	PP9	A25	I/O	Parallel port bit/Address bus bit	8
37	VCC	—	—	Power input	—
38	PP10	A26	I/O	Parallel port bit/Address bus bit	8
39	PP11	A27	I/O	Parallel port bit/Address bus bit	8
40	PP12	A28	I/O	Parallel port bit/Address bus bit	8
41	GND	—	—	Ground pin	—
42	PP13	A29	I/O	Parallel port bit/Address bus bit	8
43	PP14	A30	I/O	Parallel port bit/Address bus bit	8
44	PP15	A31	I/O	Parallel port bit/Address bus bit	8
45	VCC	—	—	Power input	—
46	SIZ0	—	I/O	Size attribute	8
47	SIZ1	—	I/O	Size attribute	8

Table 16-1. Pins 1–52 (Left, Top-to-Bottom) (Continued)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
48	GND	—	—	Ground pin	—
49	$\overline{OE}$	—	O	Output enable for chip selects	8
50	$\overline{CS0}$	—	O	Chip select	8
51	$\overline{CS1}$	—	O	Chip select	8
52	VCC	—	—	Power input	—

Table 16-2. Pins 53–104 (Bottom, Left-to-Right)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
53	GND	—	—	Ground pin	—
54	$\overline{CS2}$	—	O	Chip select	8
55	$\overline{CS3}$	—	O	Chip select	8
56	$\overline{CS4}$	—	O	Chip select	8
57	VCC	—	—	Power input	—
58	$\overline{CS5}$	—	O	Chip select	8
59	$\overline{CS6}$	—	O	Chip select	8
60	$\overline{CS7}$	—	O	Chip select	8
61	GND	—	—	Ground pin	—
62	$\overline{AS}$	—	I/O	Address strobe	8
63	R/$\overline{W}$	—	I/O	Read/$\overline{Write}$	8
64	$\overline{TA}$	—	I/O	Transfer acknowledge	8
65	VCC	—	—	Power input	—
66	$\overline{TS}$	—	I/O	Transfer start	8
67	$\overline{RSTI}$	—	I	Reset	—
68	$\overline{IRQ7}$	—	I	Interrupt request	—
69	GND	—	—	Ground pin	—
70	$\overline{IRQ5}$	$\overline{IRQ4}$	I	Interrupt request	—
71	$\overline{IRQ3}$	$\overline{IRQ6}$	I	Interrupt request	—
72	$\overline{IRQ1}$	$\overline{IRQ2}$	I	Interrupt request	—
73	VCC	—	—	Power input	—
74	$\overline{BR}$	—	O	Bus request	8
75	$\overline{BD}$	—	O	Bus driven	8
76	$\overline{BG}$	—	I	Bus grant	—
77	GND	—	—	Ground pin	—

Table 16-2. Pins 53–104 (Bottom, Left-to-Right) (Continued)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
78	TOUT1	—	O	Timer output	8
79	TOUT0	—	O	Timer output	8
80	TIN0	—	I	Timer input	—
81	VCC	—	—	Power input	—
82	TIN1	—	I	Timer input	—
83	$\overline{\text{RAS0}}$	—	O	DRAM row address strobe	16
84	$\overline{\text{RAS1}}$	—	O	DRAM row address strobe	16
85	GND	—	—	Ground pin	—
86	$\overline{\text{CAS0}}$	—	O	DRAM column address strobe	16
87	$\overline{\text{CAS1}}$	—	O	DRAM column address strobe	16
88	$\overline{\text{CAS2}}$	—	O	DRAM column address strobe	16
89	VCC	—	—	Power input	—
90	$\overline{\text{CAS3}}$	—	O	DRAM column address strobe	16
91	$\overline{\text{DRAMW}}$	—	O	DRAM write	16
92	$\overline{\text{SRAS}}$	—	O	SDRAM row address strobe	16
93	GND	—	—	Ground pin	—
94	$\overline{\text{SCAS}}$	—	O	SDRAM column address strobe	16
95	SCKE	—	O	SDRAM clock enable	16
96	$\overline{\text{BE0}}$	$\overline{\text{BWE0}}$	O	Byte enable/byte write enable	8
97	VCC	—	—	Power input	—
98	$\overline{\text{BE1}}$	$\overline{\text{BWE1}}$	O	Byte enable/byte write enable	8
99	$\overline{\text{BE2}}$	$\overline{\text{BWE2}}$	O	Byte enable/byte write enable	8
100	$\overline{\text{BE3}}$	$\overline{\text{BWE3}}$	O	Byte enable/byte write enable	8
101	GND	—	—	Ground pin	—
102	SCL	—	I/OD [1]	Serial clock line	8
103	SDA	—	I/OD [1]	Serial data line	8
104	GND	—	—	Ground pin	—

[1] OD: Open-drain output

Table 16-3. Pins 105–156 (Right, Bottom-to-Top)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
105	VCC	—	—	Power input	—
106	D31	—	I/O	Data bus	8

Table 16-3. Pins 105–156 (Right, Bottom-to-Top) (Continued)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
107	D30	—	I/O	Data bus	8
108	D29	—	I/O	Data bus	8
109	GND	—	—	Ground pin	—
110	D28	—	I/O	Data bus	8
111	D27	—	I/O	Data bus	8
112	D26	—	I/O	Data bus	8
113	VCC	—	—	Power input	—
114	D25	—	I/O	Data bus	8
115	D24	—	I/O	Data bus	8
116	D23	—	I/O	Data bus	8
117	GND	—	—	Ground pin	—
118	D22	—	I/O	Data bus	8
119	D21	—	I/O	Data bus	8
120	D20	—	I/O	Data bus	8
121	VCC	—	—	Power input	—
122	D19	—	I/O	Data bus	8
123	D18	—	I/O	Data bus	8
124	D17	—	I/O	Data bus	8
125	GND	—	—	Ground pin	—
126	D16	—	I/O	Data bus	8
127	D15	—	I/O	Data bus	8
128	D14	—	I/O	Data bus	8
129	VCC	—	—	Power input	—
130	D13	—	I/O	Data bus	8
131	D12	—	I/O	Data bus	8
132	D11	—	I/O	Data bus	8
133	GND	—	—	Ground pin	—
134	D10	—	I/O	Data bus	8
135	D9	—	I/O	Data bus	8
136	D8	—	I/O	Data bus	8
137	VCC	—	—	Power input	—
138	D7	CS_CONF2	I/O	Data bus/Chip select configuration	8
139	D6	CS_CONF1	I/O	Data bus/Chip select configuration	8
140	D5	CS_CONF0	I/O	Data bus/Chip select configuration	8
141	GND	—	—	Ground pin	—

Table 16-3. Pins 105–156 (Right, Bottom-to-Top) (Continued)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
142	D4	ADDR_CONF	I/O	Data bus/Address configuration	8
143	D3	FREQ1	I/O	Data bus/CLKIN Frequency	8
144	D2	FREQ0	I/O	Data bus/CLKIN Frequency	8
145	VCC	—	—	Power input	—
146	D1	DIVIDE1	I/O	Data bus/Divide control PCLK:BCLKO	8
147	D0	DIVIDE0	I/O	Data bus/Divide control PCLK:BCLKO	8
148	GND	—	—	Ground pin	—
149	DSCLK	$\overline{\text{TRST}}$	I	Debug serial clock/JTAG Reset	—
150	TCK	TCK	I	JTAG clock	—
151	DSO	TDO	O	Debug serial out/JTAG data out	8
152	VCC	—	—	Power input	—
153	DSI	TDI	I	Debug serial input/JTAG data in	—
154	$\overline{\text{BKPT}}$	TMS	I	Debug breakpoint/JTAG mode select	—
155	$\overline{\text{HIZ}}$	—	I	High impedance override	—
156	GND	—	—	Ground pin	—

Table 16-4. Pins 157–208 (Top, Right-to-Left)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
157	VCC	—	—	Power input	—
158	$\overline{\text{CTS1}}$	—	I	UART1 clear-to-send	—
159	$\overline{\text{RTS1}}$	—	O	UART1 request-to-send	8
160	RXD1	—	I	UART1 receive data	—
161	TXD1	—	O	UART1 transmit data	8
162	GND	—	—	Ground pin	—
163	$\overline{\text{CTS0}}$	—	I	UART0 clear-to-send	—
164	$\overline{\text{RTS0}}$	—	O	UART0 request-to-send	8
165	RXD0	—	I	UART0 receive data	—
166	TXD0	—	O	UART0 transmit data	8
167	VCC	—	—	Power input	—
168	EDGESEL	—	I	SDRAM bus clock edge select	—
169	GND	—	—	Ground pin	—
170	BCLKO	—	O	Bus clock output	16

Table 16-4. Pins 157–208 (Top, Right-to-Left) (Continued)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
171	VCC	—	—	Power input	—
172	$\overline{\text{RSTO}}$	—	O	Processor reset output	8
173	GND	—	—	Ground pin	—
174	CLKIN	—	I	Clock input	—
175	VCC	—	—	Power input	—
176	MTMOD0	—	I	JTAG/BDM select (Tie high or low)	—
177	MTMOD1	—	I	Tie high or low	—
178	PGND	—	—	PLL ground pin	—
179	NC	—	O		—
180	PVCC	—	—	Filter supply for PLL	—
181	MTMOD2	—	I	Tie high or low	—
182	MTMOD3	—	I	Tie high or low	—
183	GND	—	—	Ground pin	—
184	PSTCLK	—	O	Processor status clock	8
185	VCC	—	—	Power input	—
186	DDATA0	—	O	Debug data	8
187	DDATA1	—	O	Debug data	8
188	GND	—	—	Ground pin	—
189	DDATA2	—	O	Debug data	8
190	DDATA3	—	O	Debug data	8
191	VCC	—	—	Power input	—
192	PST0	—	O	Processor status	8
193	PST1	—	O	Processor status	8
194	GND	—	—	Ground pin	—
195	PST2	—	O	Processor status	8
196	PST3	—	O	Processor status	8
197	VCC	—	—	Power input	—
198	PP7	$\overline{\text{TIP}}$	I/O	Parallel port bit/transfer in progress	8
199	PP6	$\overline{\text{DREQ0}}$	I/O	Parallel port bit/DMA request	8
200	PP5	$\overline{\text{DREQ1}}$	I/O	Parallel port bit/DMA request	8
201	GND	—	—	Ground pin	—
202	PP4	TM2	I/O	Parallel port bit/Transfer modifier	8
203	PP3	TM1	I/O	Parallel port bit/Transfer modifier	8
204	PP2	TM0	I/O	Parallel port bit/Transfer modifier	8
205	VCC	—	—	Power input	—

Table 16-4. Pins 157–208 (Top, Right-to-Left) (Continued)

Pin		Alternate Function	I/O	Description	Drive (mA)
No	Name				
206	PP1	TT1	I/O	Parallel port bit/Transfer type	8
207	PP0	TT0	I/O	Parallel port bit/Transfer type	8
208	GND	—	—	Ground pin	—

16.3 Mechanical Diagram

Figure 16-1 is a mechanical diagram of the 208-pin QFP MCF5307.

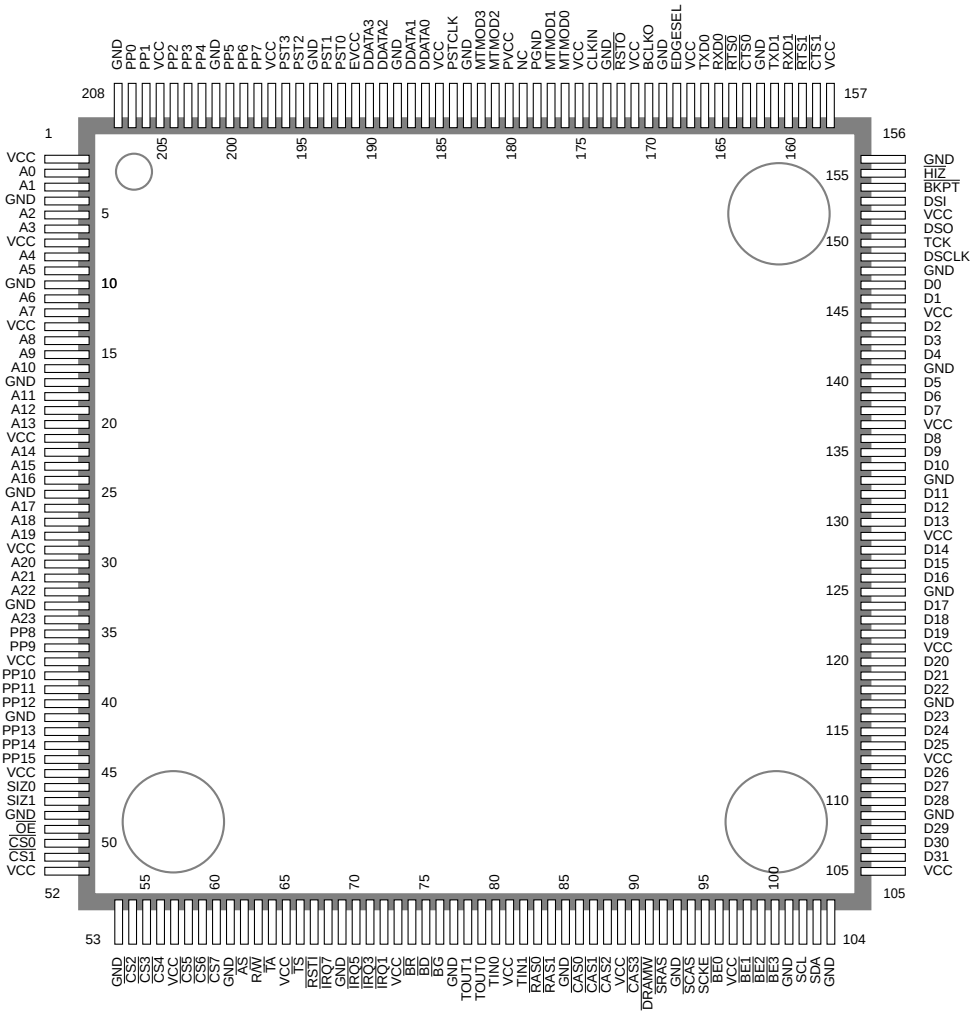


Figure 16-1. Mechanical Diagram

16.4 Case Drawing

Figure 16-2 and Figure 16-3 show the MCF5307 case drawings.

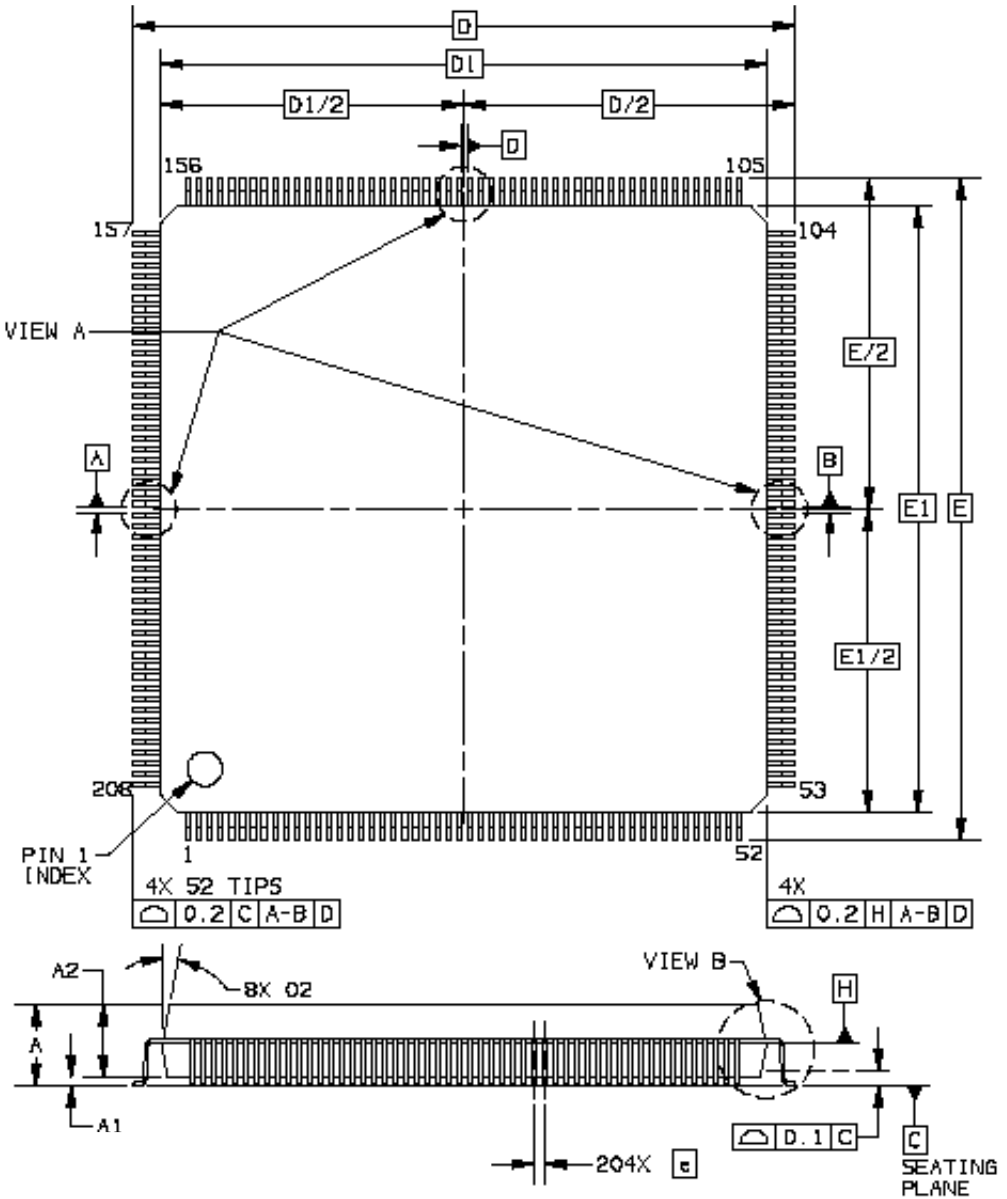
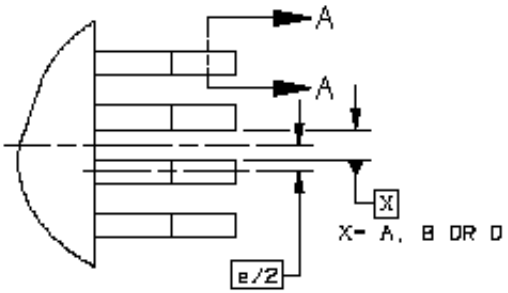
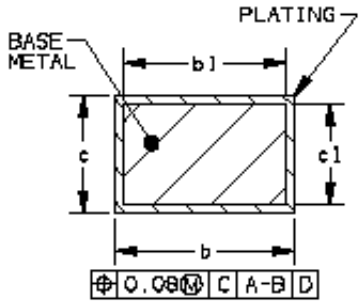


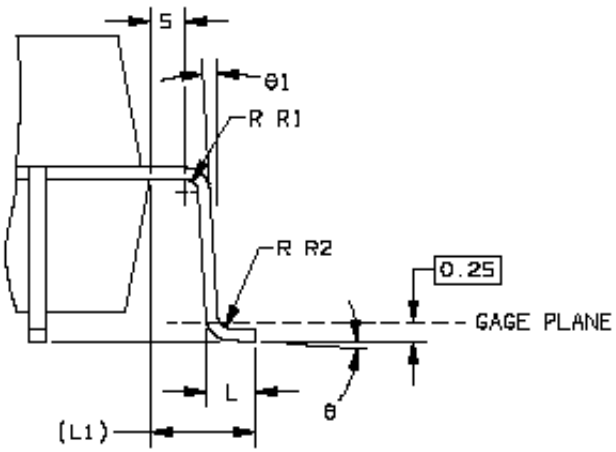
Figure 16-2. MCF5307 Case Drawing (General View)



View A: Three Places



Section A-A: 160 Places Rotated 90° CW



View B

Figure 16-3. Case Drawing (Details)

The dimensions in Figure 16-2 and Figure 16-3 are referenced in Table 16-5.

Table 16-5. Dimensions

Reference	Dimension (Millimeters)	
	Minimum	Maximum
A	—	4.10
A1	0.25	0.50
A2	3.20	3.60
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	30.60 BSC	

Table 16-5. Dimensions (Continued)

Reference	Dimension (Millimeters)	
	Minimum	Maximum
D1	28.00 BSC	
e	0.50 BSC	
E	30.60 BSC	
E1	28.00 BSC	
L	0.45	0.75
L1	1.30 REF	
R1	0.08	—
R2	0.08	0.25
S	0.20	—
ϑ	0*	8*
ϑ1	0*	—
ϑ2	5*	16*