Chapter 7
Phase-Locked Loop (PLL)

This chapter describes configuration and operation of the phase-locked loop (PLL) module. It describes in detail the registers and signals that support the PLL implementation.

7.1 Overview

The basic features of the MCF5307 PLL implementation are as follows:

- The PLL locks to the clock input (CLKIN) frequency. It provides a processor clock (PCLK) that is twice the input clock frequency and a programmable system bus clock output (BCLKO) that is 1/2, 1/3, or 1/4 the PCLK frequency.
- A buffered processor status clock (PSTCLK) is equal to the PCLK frequency, as indicated in Figure 7-1. This signal is made available for system development.

The PLL module has the following three modes of operation:

- Reset mode—In reset mode, the core/bus frequency ratio and other configuration information is sampled. At reset, the PLL asserts the reset out signal, $\overline{\text{RSTO}}$.
- Normal mode—During normal operations, the divide ratio is programmed at reset and is clock-multiplied to provide a maximum frequency of 90 MHz
- Reduced-power mode—In reduced-power mode, the high-speed processor core clocks are turned off without losing the register contents so that the system can be reenabled by an unmasked interrupt or reset.

Figure 7-1 shows the frequency relationships of PLL module clock signals.

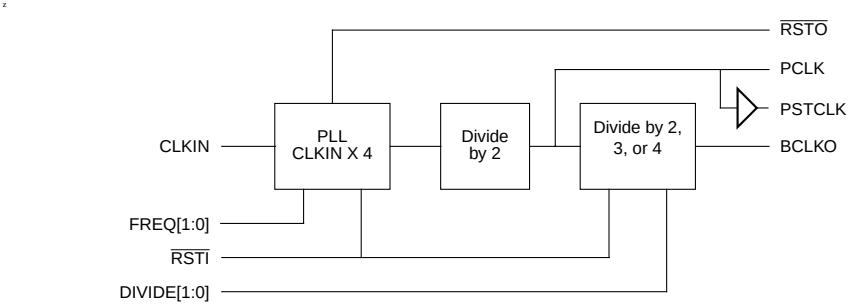


Figure 7-1. PLL Module Block Diagram

7.1.1 PLL:PCLK Ratios

The specifications for the clocks in the PLL module are summarized in Table 0-1.

Table 0-1. PLL Clock Specifications

Symbol	Description	Frequency		
—	PLL lock time	2.2 mS with CLKIN running at 45 MHz		
CLKIN	Input clock	16.67 MHz—45 MHz		
PCLK	Internal processor clock	33.34 MHz—90 MHz (CLKIN x 2)		
PSTCLK	Processor status clock	33.34 MHz—90 MHz (CLKIN x 2)		
BCLKO	Output clock	16.67 MHz—45 MHz	11.11 MHz—30 MHz	8.24 MHz—22.5 MHz
BCLKO/PCLK ratio		**1/2**	**1/3**	**1/4**

7.2 PLL Operation

The following sections provide detailed information about the three PLL modes.

7.2.1 Reset/Initialization

The PLL receives $\overline{\text{RSTI}}$ as an input directly from the pin. Additionally, signals are multiplexed with D[3:0]/FREQ[1:0]:DIVIDE[1:0] while $\overline{\text{RSTI}}$ is asserted. These signals are sampled during reset and registered by the PLL on the negation of $\overline{\text{RSTI}}$ to provide initialization information. FREQ[1:0] and DIVIDE[1:0] are used by the PLL to select the CLKIN frequency range and set the CLKIN/PCLK ratio, respectively.

7.2.2 Normal Mode

PCLK is divided to create the system bus clock, BCLKO. At reset, the logic level of DIVIDE[1:0]/D[1:0] determines the BCLKO divisor. The bus clock can be 1/2, 1/3, or 1/4 of the PCLK frequency.

7.2.3 Reduced-Power Mode

The PCLK can be turned off in a predictable manner to conserve system power. To allow fast restart of the MCF5307 processor core, the PLL continues to operate at the frequency configured at reset. PCLK is disabled using the CPU STOP instruction and resumes normal operation on interrupt, as described in Section 7.2.4, “PLL Control Register (PLLCR).”

7.2.4 PLL Control Register (PLLCR)

The PLL control register (PLLCR), Figure 7-2, provides control over the PLL.

	7	6	5	4	3	2	1	0
Field	ENBSTOP	PLLIPL			—			
Reset	0000_0000							
R/W	R/W							
Address	MBAR + 0x08							

Figure 7-2. PLL Control Register (PLLCR)

Table 7-1 describes PLLCR bits.

Table 7-1. PLLCR Field Descriptions

Bit	Name	Description
7	ENBSTOP	Enable CPU STOP instruction. Must be set for the ColdFire CPU STOP instruction to be acknowledged. Cleared at reset and must be subsequently set for the processor to enter low-power modes. Only clocks to the core are turned off because of the CPU STOP instruction. Internal modules remain clocked and can generate interrupts to restart the ColdFire core. 0 Disable CPU STOP 1 Enable CPU STOP; STOP instruction turns off clocks to the ColdFire core.
6–4	PLLIPL	PLL interrupt priority level to wake up from CPU STOP. Determines the minimum level an interrupt (decoded as an interrupt priority level) must be to waken the PLL. The PLL then turns clocks back on to the core processor and interrupt exception processing occurs. 000 Any interrupts can wake core 001 Interrupts 2–7 010 Interrupts 3–7 011 Interrupts 4–7 100 Interrupts 5–7 101 Interrupts 6–7 110 Interrupt 7 only 111 No interrupts can wake core. Any reset, including a watchdog reset, can wake the core. No PLL phase lock time is required.
3–0	—	Reserved, should be cleared.

7.3 PLL Port List

Table 7-2 describes PLL module inputs.

Table 7-2. PLL Module Input SIgnals

SIgnal	Description
CLKIN	Input clock to the PLL. Input frequency must not be changed during operation. Changes are recognized only at reset.
$\overline{\text{RSTI}}$	Active-low asynchronous input that, when asserted, indicates PLL is to enter reset mode. As long as $\overline{\text{RSTI}}$ is asserted, the PLL is held in reset and does not begin to lock.

Table 7-2. PLL Module Input SIgnals

SIgnal	Description
FREQ[1:0]	Input bus indicating the CLKIN frequency range. FREQ[1:0] are multiplexed with D[3:2] and are sampled while $\overline{\text{RSTI}}$ is asserted. FREQ[1:0] must be correctly set for proper operation. These signals do not affect CLKIN frequency but are required to set up the analog PLL to handle the input clock frequency. 00 16.6—27.999 MHz 01 28—38.999 MHz 10 39—45 MHz 11 Not used
DIVIDE[1:0]	The MCF5307 samples clock ratio encodings on the lower data bits of the bus to determine the CLKIN-to-processor clock ratio. D[1:0]/DIVIDE[1:0] support the divide-ratio combinations. 00 1/4 01 Not used 10 1/2 11 1/3

Table 7-3 describes PLL module outputs.

Table 7-3. PLL Module Output Signals

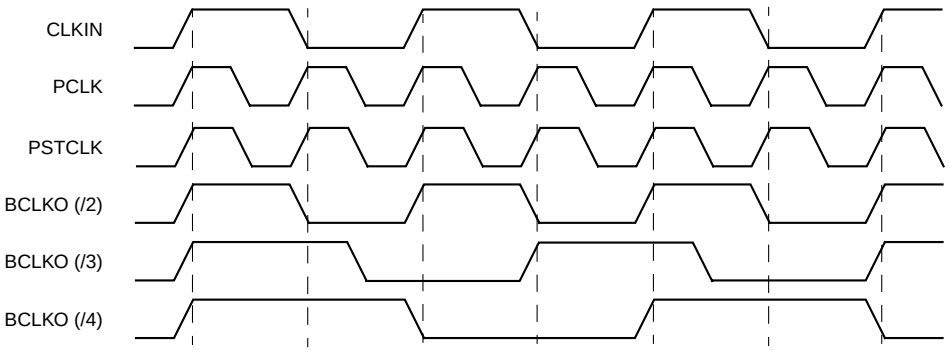
Output	Description
BCLKO	This bus clock output provides a divided version of the processor clock frequency, determined by DIVIDE[1:0].
PSTCLK	Provides a buffered processor status clock at 2X the CLKIN frequency. PSTCLK is a delayed version of PCLK. See Section 7.4.1, “PCLK, PSTCLK, and BCLKO,” and Figure 7-1.
$\overline{\text{RSTO}}$	This output provides an external reset for peripheral devices.

7.4 Timing Relationships

The MCF5307 uses CLKIN and BCLKO, which is generated by the PLL and may be used as the bus timing reference for external devices. The MCF5307 BCLKO frequency can be 1/2, 1/3, or 1/4 the processor clock. In this document, bus timings are referenced from BCLKO. Furthermore, depending on the user configuration, the BCLKO-to-processor clock ratio may differ from the CLKIN-to-processor clock ratio.

7.4.1 PCLK, PSTCLK, and BCLKO

Figure 7-3 shows the frequency relationships between PCLK, PSTCLK,CLKIN, and the three possible versions of BCLKO. This figure does not show the skew between CLKIN and PCLK, PSTCLK, and BCLKO. PSTCLK is equal to frequency of PCLK. Similarly, the skew between PCLK and BCLKO is unspecified.



NOTE: The clock signals are shown with edges aligned to show frequency relationships only. Actual signal edges have some skew between them.

Figure 7-3. CLKIN, PCLK, PSTCLK, and BCLKO Timing

7.4.2 $\overline{\text{RSTI}}$ Timing

Figure 7-4 shows PLL timing during reset. As shown, $\overline{\text{RSTI}}$ must be asserted for at least 80 CLKIN cycles to give the MCF5307 time to begin its initialization sequence. At this time, the configuration pins should be asserted (D[3:2] for FREQ[1:0] and D[1:0] for DIVIDE[1:0]), meeting the minimum setup and hold times to $\overline{\text{RSTI}}$ given in Chapter 20, “Electrical Specifications.”

On the rising edge of BCLKO before the rising edge of $\overline{\text{RSTI}}$, the data on D[7:0] is latched and the PLL begins ramping to its final operating frequency. During this ramp and lock time, BCLKO and PSTCLK are held low. The PLL locks in about 2.2 mS with a 45-MHz CLKIN, at which time BCLKOand PSTCLK begin normal operation in the specified mode. The PLL requires 100,000 CLKIN cycles to guarantee PLL lock. To allow for reset of external peripherals requiring a clock source, $\overline{\text{RSTO}}$ remains asserted for a number of BCLKO cycles, as shown in Figure 7-4.

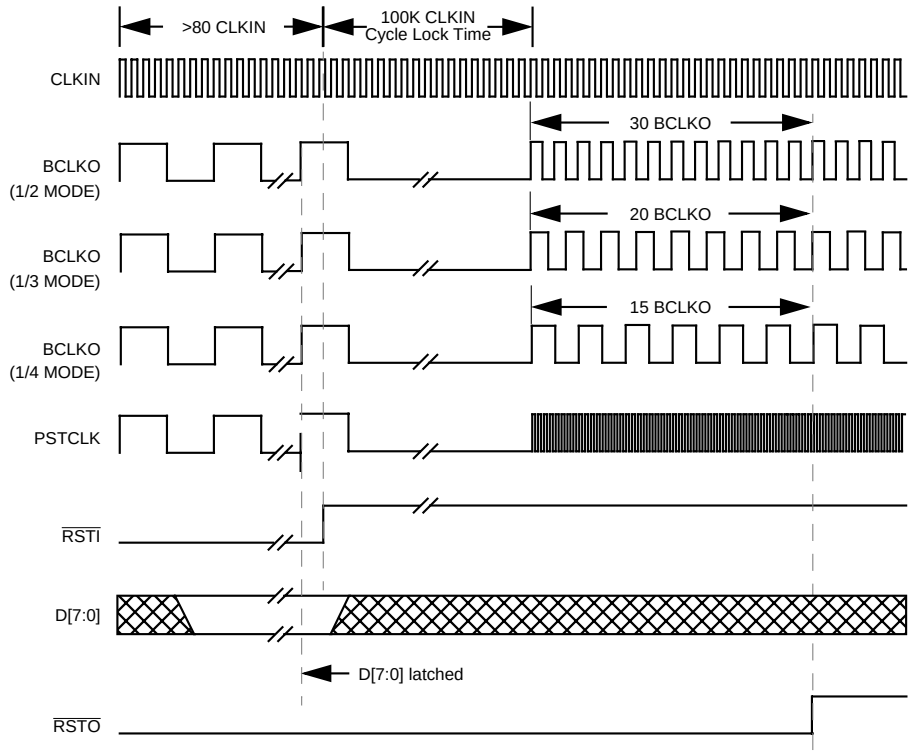


Figure 7-4. Reset and Initialization Timing

7.5 PLL Power Supply Filter Circuit

To ensure PLL stability, the power supply to the PLL power pin should be filtered using a circuit similar to the one in Figure 7-5. The circuit should be placed as close as possible to the PLL power pin to ensure maximum noise filtering.

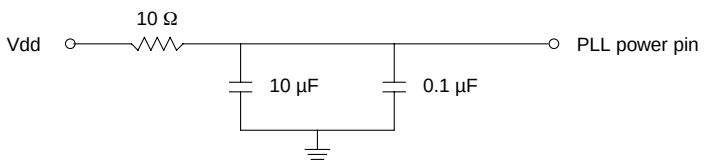


Figure 7-5. PLL Power Supply Filter Circuit