Chapter 15
Parallel Port (General-Purpose I/O)

This chapter describes the operation and programming model of the parallel port pin assignment, direction-control, and data registers. It includes a code example for setting up the parallel port.

15.1 Parallel Port Operation

The MCF5307 parallel port module has 16 signals, which are programmed as follows:

- The pin assignment register (PAR) selects the function of the 16 multiplexed pins.
- Port A data direction register (PADDR) determines whether pins configured as parallel port signals are inputs or outputs.
- The Port A data register (PADAT) shows the status of the parallel port signals.

The operations of the PAR, PADDR, and PADAT are described in the following sections.

15.1.1 Pin Assignment Register (PAR)

The pin assignment register (PAR), which is part of the system integration module (SIM), defines how each PAR bit determines each pin function, as shown in Figure 15-1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	PAR15	PAR14	PAR13	PAR12	PAR11	PAR10	PAR9	PAR8	PAR7	PAR6	PAR5	PAR4	PAR3	PAR2	PAR1	PAR0
PAR[n] = 0	PP15	PP14	PP13	PP12	PP11	PP10	PP9	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0
PAR[n] = 1	A31	A30	A29	A28	A27	A26	A25	A24	$\overline{\text{TIP}}$	$\overline{\text{DREQ0}}$	$\overline{\text{DREQ1}}$	TM2	TM1	TM0	TT1	TT0
Reset	Determined by driving D4/ADDR_CONFIG with a 1 or 0 when $\overline{\text{RSTI}}$ negates. The system is configured as PP[15:0] if D4 is low; otherwise alternate pin functions selected by PAR[n] = 1 are used.															
R/W	R/W															
Address	Address MBAR + 0x004															

Figure 15-1. Parallel Port Pin Assignment Register (PAR)

If PP[9:8]/A[25:24] are unavailable because A[25:0] are needed for external addressing, PP[15:10]/A[31:26] can be configured as general-purpose I/O. Table 15-1 summarizes MCF5307 parallel port pins, described in detail in Chapter 17, “Signal Descriptions.”

Table 15-1. Parallel Port Pin Descriptions

Pin	Description
PP[15:8]/ A[31:24]	MSB of the address bus/parallel port. Programmed through PAR[15–8]. If a PAR bit is 0, the associated pin functions as a parallel port signal. If a bit is 1, the pin functions as an address bus signal. If all pins are address signals, as much as 4 Gbytes of memory space are available.
$\overline{\text{TIP}}$/PP7	Transfer-in-progress output/parallel port bit 7. Programmed through PAR[7]. Assertion indicates a bus transfer is in progress; negation indicates an idle bus cycle if the bus is still granted to the processor. Note that $\overline{\text{TIP}}$ is held asserted on back-to-back bus cycles.
$\overline{\text{DREQ}}$[1:0]/ PP[6:5]	DMA request inputs/two bits of the parallel port. Programmed through PAR[6–5]. These inputs are asserted by a peripheral device to request a DMA transfer.
TM[2:0]/ PP[4:2]]	Transfer type outputs/parallel port bits 4–2. Programmed through PAR[4–2]. For DMA transfers, these signals provide acknowledge information. For emulation transfers, TM[2:0] indicate user or data transfer types. For CPU space transfers, TM[2:0] are low. For interrupt acknowledge transfers, TM[2:0] carry the interrupt level being acknowledged.
TT[1:0]/ PP[1:0]	Transfer type outputs/parallel port bits 1–0. Programmed through PAR[1–0]. When the MCF5307 is bus master, it outputs these signals. They indicate the current bus access type.

15.1.2 Port A Data Direction Register (PADDR)

The PADDR determines the signal direction of each parallel port pin programmed as a general-purpose I/O port in the PAR.

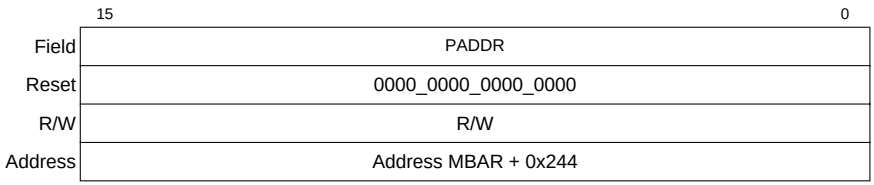

Figure 15-2. Port A Data Direction Register (PADDR)

Table 15-2 describes PADDR fields.

Table 15-2. PADDR Field Description

Bits	Name	Description
15–0	PADDR	Data direction bits. Each data direction bit selects the direction of the signal as follows: 0 Signal is defined as an input. 1 Signal is defined as an output.

15.1.3 Port A Data Register (PADAT)

The PADAT value for inputs corresponds to the logic level at the pin; for outputs, the value corresponds to the logic level driven onto the pin. Note the following:

- PADAT has no effect on pins not configured for general-purpose I/O.
- PADAT settings do not affect inputs. PADAT bit values determine the corresponding logic levels of pins configured as outputs.

- PADAT can be written to anytime. A read from PADAT returns values of corresponding pins configured as general-purpose I/O in the PAR and designated as inputs by the PADDR.

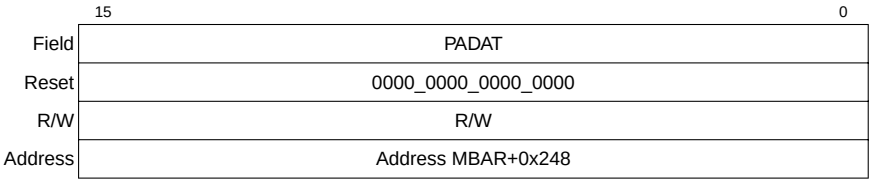

Figure 15-3. Port A Data Register (PADAT)

Table 15-3 shows relationships between PADAT bits and parallel port pins when PADAT is accessed. The effect differs when the parallel port pin is an input or output.

The following results occur when a parallel port pin is configured as an input:

- When the PADAT is read, the value returned is the logic value on the pin.
- When the PADAT is written, the register contents are updated without affecting the logic value on the pin.

The following results occur when a parallel port pin is configured as an output:

- When the PADAT is read, the register contents are returned and the pin is the logic value of the register.
- When the PADAT is written, the register contents are updated and the pin is the logic value of the register.

These relationships are also described in Table 15-3.

Table 15-3. Relationship between PADAT Register and Parallel Port Pin (PP)

PP Status	PADAT R/W	Effect on PADAT	Effect on PP
Input	Read	Register bit value is the pin's logic value	No effect. Source of logic value
	Write	Register contents updated	No effect on the logic value at the pin
Output	Read	Register contents are returned	Pin is the logic value of the register bit
	Write	Register contents updated	Pin is the logic value of the register bit

NOTE:

Although external devices cannot access the MCF5307's on-chip memories or MBAR, they can access any parallel port module registers in the SIM.

15.1.4 Code Example

The following code example shows how to set up the parallel port. Here, PP[7:0] are general-purpose I/O, PP[3:0] are inputs, and PP[7:4] are outputs.

```
MBARx   EQU   0x00010000
PAR     EQU   MBARx+0x004
PADDR   EQU   MBARx+0x244
PADAT   EQU   MBARx+0x248

move.l  #MBARx,D0      ;because MBAR is an internal register, MBARx is used as
movec   D0, MBAR       ;label for the memory map address
move.w  #0x00FF,D0
move.w  D0,PAR         ;set up the PAR. PP[7:0] set up as I/O
move.w  #0x00F0,D0
move.w  D0,PADDR       ;set PP[7:4] as outputs; PP[3:0] as inputs
move.b  #0xA0,D0
move.b  D0,PADAT       ;0xA0 written into PADAT; PP[7:4] being outputs,
                       ;PP[7:4] becomes 1010; i.e. PP7, PP5 = 1 and
                       ;PP6, PP4 = 0
```