About This Book

The primary objective of this user's manual is to define the functionality of the MCF5307 processors for use by software and hardware developers.

The information in this book is subject to change without notice, as described in the disclaimers on the title page of this book. As with any technical documentation, it is the readers' responsibility to be sure they are using the most recent version of the documentation.

To locate any published errata or updates for this document, refer to the world-wide web at http://www.motorola.com/coldfire.

Audience

This manual is intended for system software and hardware developers and applications programmers who want to develop products for the MCF5307. It is assumed that the reader understands operating systems, microprocessor system design, basic principles of software and hardware, and basic details of the ColdFire architecture.

Organization

Following is a summary and a brief description of the major sections of this manual:

- Chapter 1, "Overview," includes general descriptions of the modules and features incorporated in the MCF5307, focussing in particular on new features.
- Part I is intended for system designers who need to understand the operation of the MCF5307 ColdFire core.
  - — Chapter 2, "ColdFire Core," provides an overview of the microprocessor core of the MCF5307. The chapter begins with a description of enhancements from the V2 ColdFire core, and then fully describes the V3 programming model as it is implemented on the MCF5307. It also includes a full description of exception handling, data formats, an instruction set summary, and a table of instruction timings.
  - — Chapter 3, "Hardware Multiply/Accumulate (MAC) Unit," describes the MCF5307 multiply/accumulate unit, which executes integer multiply, multiply-accumulate, and miscellaneous register instructions. The MAC is integrated into the operand execution pipeline (OEP).

— Chapter 4, “Local Memory.” This chapter describes the MCF5307 implementation of the ColdFire V3 local memory specification. It consists of the two following major sections.

– Section 4.2, “SRAM Overview,” describes the MCF5307 on-chip static RAM (SRAM) implementation. It covers general operations, configuration, and initialization. It also provides information and examples showing how to minimize power consumption when using the SRAM.

– Section 4.7, “Cache Overview,” describes the MCF5307 cache implementation, including organization, configuration, and coherency. It describes cache operations and how the cache interacts with other memory structures.

— Chapter 5, “Debug Support,” describes the Revision C enhanced hardware debug support in the MCF5307. This revision of the ColdFire debug architecture encompasses earlier revisions.

- Part II, “System Integration Module (SIM),” describes the system integration module, which provides overall control of the bus and serves as the interface between the ColdFire core processor complex and internal peripheral devices. It includes a general description of the SIM and individual chapters that describe components of the SIM, such as the phase-lock loop (PLL) timing source, interrupt controller for peripherals, configuration and operation of chip selects, and the SDRAM controller.

— Chapter 6, “SIM Overview,” describes the SIM programming model, bus arbitration, and system-protection functions for the MCF5307.

— Chapter 7, “Phase-Locked Loop (PLL),” describes configuration and operation of the PLL module. It describes in detail the registers and signals that support the PLL implementation.

— Chapter 8, “I^2C Module,” describes the MCF5307 I^2C module, including I^2C protocol, clock synchronization, and the registers in the I^2C programing model. It also provides extensive programming examples.

— Chapter 9, “Interrupt Controller,” describes operation of the interrupt controller portion of the SIM. Includes descriptions of the registers in the interrupt controller memory map and the interrupt priority scheme.

— Chapter 10, “Chip-Select Module,” describes the MCF5307 chip-select implementation, including the operation and programming model, which includes the chip-select address, mask, and control registers.

— Chapter 11, “Synchronous/Asynchronous DRAM Controller Module,” describes configuration and operation of the synchronous/asynchronous DRAM controller component of the SIM. It begins with a general description and brief glossary, and includes a description of signals involved in DRAM operations. The remainder of the chapter is divided between descriptions of asynchronous and synchronous operations.

- Part III, “Peripheral Module,” describes the operation and configuration of the MCF5307 DMA, timer, UART, and parallel port modules, and describes how they interface with the system integration unit, described in Part II.
  - — Chapter 12, “DMA Controller Module,” provides an overview of the DMA controller module and describes in detail its signals and registers. The latter sections of this chapter describe operations, features, and supported data transfer modes in detail, showing timing diagrams for various operations.
  - — Chapter 13, “Timer Module,” describes configuration and operation of the two general-purpose timer modules, timer 0 and timer 1. It includes programming examples.
  - — Chapter 14, “UART Modules,” describes the use of the universal asynchronous/synchronous receiver/transmitters (UARTs) implemented on the MCF5307 and includes programming examples.
  - — Chapter 15, “Parallel Port (General-Purpose I/O),” describes the operation and programming model of the parallel port pin assignment, direction-control, and data registers. It includes a code example for setting up the parallel port.
- Part IV, “Hardware Interface,” provides a pinout and both electrical and functional descriptions of the MCF5307 signals. It also describes how these signals interact to support the variety of bus operations shown in timing diagrams.
  - — Chapter 16, “Mechanical Data,” provides a functional pin listing and package diagram for the MCF5307.
  - — Chapter 17, “Signal Descriptions,” provides an alphabetical listing of MCF5307 signals. This chapter describes the MCF5307 signals. In particular, it shows which are inputs or outputs, how they are multiplexed, which signals require pull-up resistors, and the state of each signal at reset.
  - — Chapter 18, “Bus Operation,” describes data transfers, error conditions, bus arbitration, and reset operations. It describes transfers initiated by the MCF5307 and by an external bus master, and includes detailed timing diagrams showing the interaction of signals in supported bus operations. Note that Chapter 11, “Synchronous/Asynchronous DRAM Controller Module,” describes DRAM cycles.
  - — Chapter 19, “IEEE 1149.1 Test Access Port (JTAG),” describes configuration and operation of the MCF5307 JTAG test implementation. It describes the use of JTAG instructions and provides information on how to disable JTAG functionality.
  - — Chapter 20, “Electrical Specifications,” describes AC and DC electrical specifications and thermal characteristics for the MCF5307. Because additional speeds may have become available since the publication of this book, consult Motorola’s ColdFire web page, http://www.motorola.com/coldfire, to confirm that this is the latest information.

This manual includes the following appendix:

- Appendix A, “List of Memory Maps,” lists the entire address-map for MCF5307 memory-mapped registers.

This manual also includes a glossary and an index.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the ColdFire architecture.

General Information

The following documentation provides useful information about the ColdFire architecture and computer architecture in general:

ColdFire Documentation

The ColdFire documentation is available from the sources listed on the back cover of this manual. Document order numbers are included in parentheses for ease in ordering.

- *ColdFire Programmers Reference Manual, R1.0* (MCF5200PRM/AD)
- User’s manuals—These books provide details about individual ColdFire implementations and are intended to be used in conjunction with *The ColdFire Programmers Reference Manual*. These include the following:
  - *ColdFire MCF5102 User’s Manual* (MCF5102UM/AD)
  - *ColdFire MCF5202 User’s Manual* (MCF5202UM/AD)
  - *ColdFire MCF5204 User’s Manual* (MCF5204UM/AD)
  - *ColdFire MCF5206 User’s Manual* (MCF5206EUM/AD)
  - *ColdFire MCF5206E User’s Manual* (MCF5206EUM/AD)
- *ColdFire Programmers Reference Manual, R1.0* (MCF5200PRM/AD)
- *Using Microprocessors and Microcomputers: The Motorola Family*, William C. Wray, Ross Bannatyne, Joseph D. Greenfield

Additional literature on ColdFire implementations is being released as new processors become available. For a current list of ColdFire documentation, refer to the World Wide Web at http://www.motorola.com/ColdFire/.

Conventions

This document uses the following notational conventions:

MNEMONICS	In text, instruction mnemonics are shown in uppercase.
`mnemonics`	In code and tables, instruction mnemonics are shown in lowercase.

italics	Italics indicate variable command parameters. Book titles in text are set in italics.
0x0	Prefix to denote hexadecimal number
0b0	Prefix to denote binary number
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields, or ranges appear in brackets. For example, RAMBAR[BA] identifies the base address field in the RAM base address register.
nibble	A 4-bit data unit
byte	An 8-bit data unit
word	A 16-bit data unit
longword	A 32-bit data unit
x	In some contexts, such as signal encodings, x indicates a don’t care.
n	Used to express an undefined numerical value
¬	NOT logical operator
&	AND logical operator
|	OR logical operator

Acronyms and Abbreviations

Table i lists acronyms and abbreviations used in this document.

Table i. Acronyms and Abbreviated Terms

Term	Meaning
ADC	Analog-to-digital conversion
ALU	Arithmetic logic unit
AVEC	Autovector
BDM	Background debug mode
BIST	Built-in self test
BSDL	Boundary-scan description language
CODEC	Code/decode
DAC	Digital-to-analog conversion
DMA	Direct memory access
DSP	Digital signal processing
EA	Effective address
EDO	Extended data output (DRAM)
FIFO	First-in, first-out

Table i. Acronyms and Abbreviated Terms (Continued)

Term	Meaning
GPIO	General-purpose I/O
I^2C	Inter-integrated circuit
IEEE	Institute for Electrical and Electronics Engineers
IFP	Instruction fetch pipeline
IPL	Interrupt priority level
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LIFO	Last-in, first-out
LRU	Least recently used
LSB	Least-significant byte
lsb	Least-significant bit
MAC	Multiple accumulate unit
MBAR	Memory base address register
MSB	Most-significant byte
msb	Most-significant bit
Mux	Multiplex
NOP	No operation
OEP	Operand execution pipeline
PC	Program counter
PCLK	Processor clock
PLL	Phase-locked loop
PLRU	Pseudo least recently used
POR	Power-on reset
PQFP	Plastic quad flat pack
RISC	Reduced instruction set computing
Rx	Receive
SIM	System integration module
SOF	Start of frame
TAP	Test access port
TTL	Transistor-to-transistor logic
Tx	Transmit
UART	Universal asynchronous/synchronous receiver transmitter

Terminology and Notational Conventions

Table ii shows notational conventions used throughout this document.

Table ii Notational Conventions

Instruction	Operand Syntax
Opcode Wildcard	
cc	Logical condition (example: NE for not equal)
Register Specifications	
An	Any address register n (example: A3 is address register 3)
Ay,Ax	Source and destination address registers, respectively
Dn	Any data register n (example: D5 is data register 5)
Dy,Dx	Source and destination data registers, respectively
Rc	Any control register (example VBR is the vector base register)
Rm	MAC registers (ACC, MAC, MASK)
Rn	Any address or data register
Rw	Destination register w (used for MAC instructions only)
Ry,Rx	Any source and destination registers, respectively
Xi	index register i (can be an address or data register: Ai, Di)
Register Names	
ACC	MAC accumulator register
CCR	Condition code register (lower byte of SR)
MACSR	MAC status register
MASK	MAC mask register
PC	Program counter
SR	Status register
Port Name	
PSTDDATA	Processor status/debug data port
Miscellaneous Operands	
#<data>	Immediate data following the 16-bit operation word of the instruction
<ea>	Effective address
<ea>y,<ea>x	Source and destination effective addresses, respectively
<label>	Assembly language program label
<list>	List of registers for MOVEM instruction (example: D3–D0)
<shift>	Shift operation: shift left (<<), shift right (>>)
<size>	Operand data size: byte (B), word (W), longword (L)
bc	Both instruction and data caches
dc	Data cache

Table ii Notational Conventions (Continued)

Instruction	Operand Syntax
ic	Instruction cache
# <vector>	Identifies the 4-bit vector number for trap instructions
<>	identifies an indirect data address referencing memory
<xxx>	identifies an absolute address referencing memory
dn	Signal displacement value, n bits wide (example: d16 is a 16-bit displacement)
SF	Scale factor (x1, x2, x4 for indexed addressing mode, <<1n>> for MAC operations)
Operations	
+	Arithmetic addition or postincrement indicator
–	Arithmetic subtraction or predecrement indicator
x	Arithmetic multiplication
/	Arithmetic division
~	Invert; operand is logically complemented
&	Logical AND
|	Logical OR
^	Logical exclusive OR
<<	Shift left (example: D0 << 3 is shift D0 left 3 bits)
>>	Shift right (example: D0 >> 3 is shift D0 right 3 bits)
→	Source operand is moved to destination operand
←→	Two operands are exchanged
sign-extended	All bits of the upper portion are made equal to the high-order bit of the lower portion
If <condition> then <operations> else <operations>	Test the condition. If true, the operations after ‘then’ are performed. If the condition is false and the optional ‘else’ clause is present, the operations after ‘else’ are performed. If the condition is false and else is omitted, the instruction performs no operation. Refer to the Bcc instruction description as an example.
Subfields and Qualifiers	
{}	Optional operation
()	Identifies an indirect address
d_n	Displacement value, n-bits wide (example: d_{16} is a 16-bit displacement)
Address	Calculated effective address (pointer)
Bit	Bit selection (example: Bit 3 of D0)
lsb	Least significant bit (example: lsb of D0)
LSB	Least significant byte
LSW	Least significant word
msb	Most significant bit
MSB	Most significant byte
MSW	Most significant word

Table ii Notational Conventions (Continued)

Instruction	Operand Syntax
Condition Code Register Bit Names	
C	Carry
N	Negative
V	Overflow
X	Extend
Z	Zero