Chapter 17
Signal Descriptions

This chapter describes MCF5307 signals. It includes an alphabetical listing of signals, showing multiplexing, whether it is an input or output to the MCF5307, the state at reset, and whether a pull-up resistor should be used. The following chapter, Chapter 18, “Bus Operation,” describes how these signals interact.

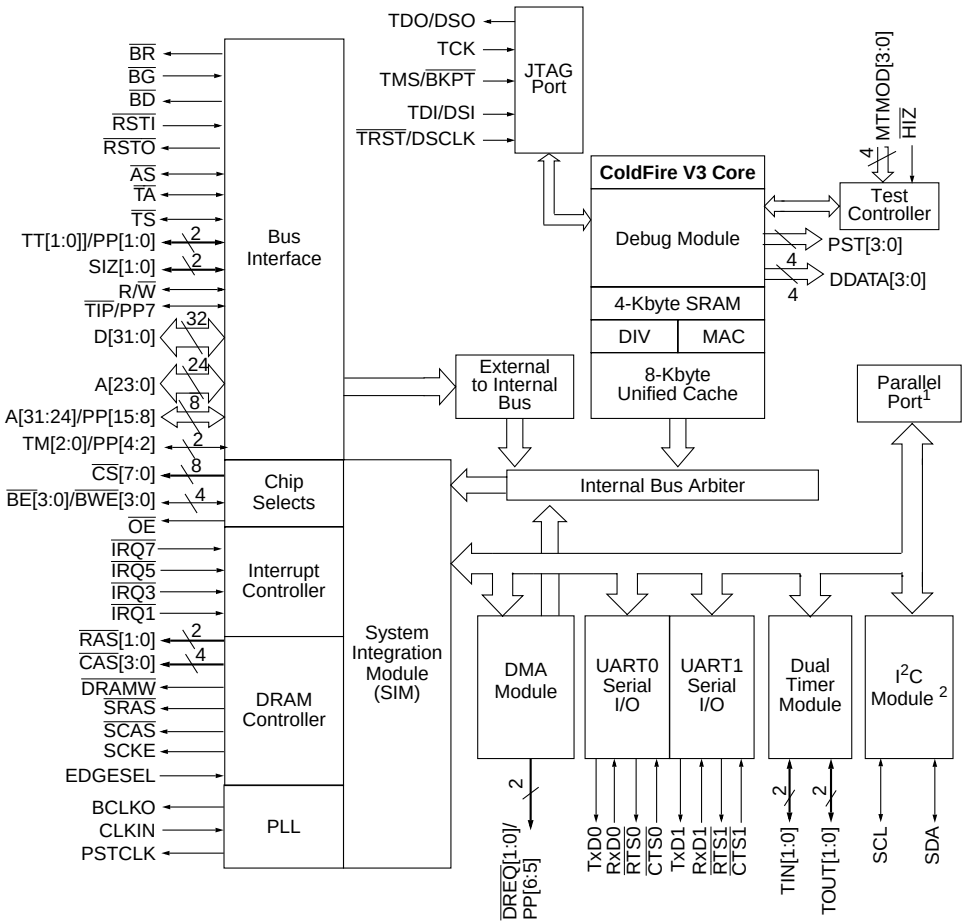
NOTE:

The terms ‘assertion’ and ‘negation’ are used to avoid confusion when dealing with a mixture of active-low and active-high signals. The term ‘asserted’ indicates that a signal is active, independent of the voltage level. The term ‘negated’ indicates that a signal is inactive.

Active-low signals, such as $\overline{\text{SRAS}}$ and $\overline{\text{TA}}$, are indicated with an overbar.

17.1 Overview

Figure 17-1 shows the block diagram of the MCF5307 with the signal interface.



[1] Note: Parallel port pins (PPn) are multiplexed with other bus functions as shown.
[2] I²C is a Philips proprietary interface

Figure 17-1. MCF5307 Block Diagram with Signal Interfaces

Table 17-1 lists the MCF5307 signals grouped by functionality.

Table 17-1. MCF5307 Signal Index

Signal Name	Abbreviation	Function	I/O	Reset	Pull-Up	Page
Section 17.2, "MCF5307 Bus Signals"						17-7
Address	A[31:0]	32-bit address bus. A[4:2] indicate the interrupt level for external interrupts.	I/O	Three state		17-7
Data	D[31:0]	Data bus. D[7:0] are loaded at reset for bus configuration.	I/O	Three state		17-8
Read/Write	R/$\overline{W}$	Identifies read and write transfers	I/O	Three state	Up	17-8
Size	SIZ[1:0]	Indicates the data transfer size	I/O	Three state		17-8
Transfer start	$\overline{TS}$	Indicates the start of a bus transfer	I/O	Three state		17-9
Address strobe	$\overline{AS}$	Indicates a bus cycle has been initiated and address is stable	I/O	Three state	Up	17-9
Transfer acknowledge	$\overline{TA}$	Assertion terminates transfer synchronously	I/O	Three state	Up	17-9
Transfer in progress	$\overline{TIP}$/PP7	Indicates a bus cycle is in progress; multiplexed with PP7	O	Parallel port		17-10
Transfer type	TT[1:0]	Indicates transfer type: normal, CPU space, emulator mode, or DMA; multiplexed with PP[1:0]	O	Parallel port		17-10
Transfer modifier	TM[2:0]	Provides transfer modifier information; Multiplexed with PP[4:2].	O	Parallel port		17-10
Section 17.3, "Interrupt Control Signals"						17-12
Interrupt request	$\overline{IRQ7}$, $\overline{IRQ5}$, $\overline{IRQ3}$, $\overline{IRQ1}$	Four external interrupts are set to default levels 1,3,5,7; user-alterable.	I	—	Up	17-12
Section 17.4, "Bus Arbitration Signals"						17-12
Bus request	$\overline{BR}$	Indicates processor needs bus	O	High		17-12
Bus grant	$\overline{BG}$	Arbiter asserts to grant mastership.	I	—	Note [1]	17-12
Bus driven	$\overline{BD}$	Indicates processor is driving bus	O	High		17-13
Section 17.5, "Clock and Reset Signals"						17-13
Reset in	$\overline{RSTI}$	Processor reset input	I	—	Up	17-13
Clock input	CLKIN	Input used to clock internal logic	I	—		17-13
Bus clock out	BCLKO	Bus clock reference output	O	—		17-13
Reset out	$\overline{RSTO}$	Processor reset output	O	Low		17-13
Auto-acknowledge configuration [2]	AA_CONFIG	Controls auto acknowledge timing for $\overline{CS0}$ at reset	I	—		17-14
Port size configuration [2]	PS_CONFIG[1:0]	Controls port size for $\overline{CS0}$ at reset	I	—	User cfg	17-14
Address configuration [2]	ADDR_CONFIG	Programs parallel I/O ports	I	—	User cfg	17-14

Table 17-1. MCF5307 Signal Index (Continued)

Signal Name	Abbreviation	Function	I/O	Reset	Pull-Up	Page
Frequency control PLL	FREQ[1:0]	Indicates CLKIN frequency range.	I			17-15
Divide control PCLK to BCLKO	DIVIDE[1:0]	Indicates the BCLKO/PSTCLK ratio.	I			17-15
Section 17.6, "Chip-Select Module Signals"						17-15
Chip selects[7:0]	$\overline{CS}$[7:0]	Enables peripherals at programmed addresses; $\overline{CS0}$ provides boot ROM selection.	O	High		17-16
Byte enable[3:0]/ Byte write enable[3:0]	$\overline{BE}$[3:0]/ $\overline{BWE}$[3:0]	$\overline{BE}$[3:0] select bytes in memory.	O	High		17-16
Output enable	$\overline{OE}$	Output enable for chip select read cycles	O	High		17-16
Section 17.7, "DRAM Controller Signals"						17-16
Row address strobe	$\overline{RAS}$[1:0]	DRAM row address strobe	O	High		17-16
Column address strobe	$\overline{CAS}$[3:0]	DRAM column address strobe	O	High		17-16
DRAM write	$\overline{DRAMW}$	Asserted for DRAM write; negated for DRAM read	O	High		17-17
Synchronous column address strobe	$\overline{SCAS}$	SDRAM column address strobe	O	High		17-17
Synchronous row address strobe	$\overline{SRAS}$	SDRAM row address strobe	O	High		17-17
Synchronous clock enable	SCKE	Clock enable for external SDRAM	O	Low		17-17
Synchronous edge select	EDGESEL	Timing select for external SDRAM	I	—	User cfg	17-17
Section 17.8, "DMA Controller Module Signals"						17-17
DMA request	$\overline{DREQ}$[1:0]	External DMA transfer request; multiplexed with PP[6:5]	I	—		17-18
Section 17.9, "Serial Module Signals"						17-18
Receive data	RxD[1:0]	Receive serial data input for UART	I	—		17-18
Transmit data	TxD[1:0]	Transmit serial data output for UART	O	High		17-18
Request-to-send	$\overline{RTS}$[1:0]	UART asserts when ready to receive data query.	O	High		17-18
Clear-to-send	$\overline{CTS}$[1:0]	Signals UART that data can be sent to peripheral	I	—		17-18
Section 17.10, "Timer Module Signals"						17-18
Timer input	TIN[1:0]	Clock input to timer or trigger to timer value capture logic	I	—		17-19
Timer outputs	TOUT[1:0]	Outputs waveform or pulse.	O	High		17-19
Section 17.11, "Parallel I/O Port (PP[15:0])"						17-19

Table 17-1. MCF5307 Signal Index (Continued)

Signal Name	Abbreviation	Function	I/O	Reset	Pull-Up	Page
Parallel port	PP[15:0]	Interfaces with I/O; multiplexed with bus address and attribute signals.	I/O	Input		17-19
Section 17.12, "I²C Module Signals"						17-19
Serial clock line	SCL	Clock signal for I²C operation	I/O	Open drain	Up	17-19
Serial data line	SDA	Serial data port for I²C operation	I/O	Open drain	Up	17-19
Section 17.13, "Debug and Test Signals"						17-20
Motorola test mode	MTMOD0	Puts processor in functional or emulator mode	I	—	User cfg	17-20
Motorola test mode	MTMOD[3:1]	Reserved	I	—	Down	17-20
High impedance	$\overline{\text{HIZ}}$	Assertion three-states all outputs	I	—	Up	17-20
Processor clock out	PSTCLK	Output clock used for PSTDDATA	O	—		17-20
Processor status	PST[3:0]	Displays captured processor data .	O	Driven		17-20
Debug data	DDATA[3:0]	Displays captured processor data and breakpoint status.	O	Driven		17-20
Section 17.14, "Debug Module/JTAG Signals"						17-21
Test clock	TCK	Clock signal for IEEE 1149.1 JTAG	I	—	Low	17-23
Test reset/ Development serial clock	$\overline{\text{TRST}}$/DSCLK	Asynchronous reset for JTAG; debug module clock input	I	—	Up	17-21
Test mode select/ Breakpoint	TMS/$\overline{\text{BKPT}}$	TMS (JTAG)/hardware breakpoint (debug)	I	—	Up	17-22
Test data input/ Development serial input	TDI/DSI	Multiplexed serial input for the JTAG or background debug module	I	—	Up	17-22
Test data output/ Development serial output	TDO/DSO	Multiplexed serial output for the JTAG or background debug module	O	Driven		17-22

1 If there is no arbiter, $\overline{\text{BG}}$ should be tied low; otherwise, it should be negated.

2 These data pins are sampled at reset for configuration.

Table 17-2 lists signals in alphabetical order by abbreviated name.

Table 17-2. MCF507 Alphabetical Signal Index

Abbreviation	Signal Name	Function	I/O	Page
AA_CONFIG	Auto-acknowledge configuration	Clock/reset	I	17-14
ADDR_CONFIG	Address configuration	Clock/reset	I	17-14
$\overline{\text{AS}}$	Address strobe	Bus	I/O	17-9
A[31:0]	Address	Bus	I/O	17-7

Table 17-2. MCF507 Alphabetical Signal Index (Continued)

Abbreviation	Signal Name	Function	I/O	Page
BCLKO	Bus clock out	Clock/reset	O	17-13
$\overline{BD}$	Bus driven	Bus arbitration	O	17-13
$\overline{BE}$[3:0]/$\overline{BWE}$[3:0]	Byte enable[3:0]/Byte write enable[3:0]	Chip select	O	17-16
$\overline{BG}$	Bus grant	Bus arbitration	I	17-12
$\overline{BR}$	Bus request	Bus arbitration	O	17-12
$\overline{CAS}$[3:0]	Column address strobe	DRAM	O	17-16
CLKIN	Clock input	Clock/reset	I	17-13
$\overline{CS}$[7:0]	Chip selects[7:0]	UART	O	17-16
$\overline{CTS}$[1:0]	Clear-to-send	Serial module	I	17-18
DDATA[3:0]	Debug data	Debug	O	17-20
		Clock/Reset	I	17-15
$\overline{DRAMW}$	DRAM write	DRAM	O	17-17
$\overline{DREQ}$[1:0]	DMA request	DMA	I	17-18
D[31:0]	Data	Bus	I/O	17-8
EDGESEL	Sync edge select	DRAM	I	17-17
		Clock/Reset	I	17-15
$\overline{HIZ}$	High impedance	Debug	I	17-20
$\overline{IRQ7}$, $\overline{IRQ5}$, $\overline{IRQ3}$, $\overline{IRQ1}$	Interrupt request	Interrupt control	I	17-12
MTMOD[3:0]	Motorola test mode	Debug	I	17-20
$\overline{OE}$	Output enable	Chip select	O	17-16
PP[15:0]	Parallel port	Parallel port	I/O	17-19
PSTCLK	Processor clock out	Debug	O	17-20
PST[:0]	Processor status	Debug	O	17-20
PS_CONFIG[1:0]	Port size configuration	Clock/reset	I	17-14
R/$\overline{W}$	Read/Write	Bus	I/O	17-8
$\overline{RAS}$[1:0]	Row address strobe	DRAM	O	17-16
$\overline{RSTI}$	Reset In	Clock/reset	I	17-13
$\overline{RSTO}$	Reset Out	Clock/reset	O	17-13
$\overline{RTS}$[1:0]	Request-to-send	Serial module	O	17-18
RxD[1:0]	Receive data	Serial module	I	17-18
$\overline{SCAS}$	Synchronous column address strobe	DRAM	O	17-17
SCKE	Synchronous clock enable	DRAM	O	17-17
SCL	Serial clock line	I^2C	I/O	17-19
SDA	Serial data line	I^2C	I/O	17-19
SIZ[1:0]	Size	Bus	I/O	17-8

Table 17-2. MCF507 Alphabetical Signal Index (Continued)

Abbreviation	Signal Name	Function	I/O	Page
$\overline{\text{SRAS}}$	Synchronous row address strobe	DRAM	O	17-17
$\overline{\text{TA}}$	Transfer acknowledge	Bus	I/O	17-9
TCK	Test clock	JTAG	I	17-23
TDI/DSI	Test data input/Development serial input	JTAG	I	17-22
TDO/DSO	Test data output/Development serial output	JTAG	O	17-22
TIN[1:0]	Timer input	Timer	I	17-19
$\overline{\text{TIP}}$	Transfer in progress	Bus	O	17-10
TMS/$\overline{\text{BKPT}}$	Test mode select/Breakpoint	JTAG	I	17-22
TM[2:0]	Transfer modifier	Bus	O	17-10
TOUT[1:0]	Timer outputs	Timer	O	17-19
$\overline{\text{TRST}}$/DSCLK	Test reset/Development serial clock	JTAG	I	17-21
$\overline{\text{TS}}$	Transfer start	Bus	I/O	17-9
TT[1:0]	Transfer type	Bus	O	17-10
TxD[1:0]	Transmit data	Serial module	O	17-18

17.2 MCF5307 Bus Signals

The bus signals provide the external bus interface to the MCF5307.

17.2.1 Address Bus

The address bus provides the address of the byte or most-significant byte (MSB) of the word or longword being transferred. The address lines also serve as the DRAM addressing, providing multiplexed row and column address signals. When an external device has ownership of the MCF5307 bus, the device must drive the address bus and assert $\overline{\text{TS}}$ or $\overline{\text{AS}}$ to indicate the start of a bus cycle. During an interrupt acknowledge access, A[4:2] indicate the interrupt level being acknowledged.

17.2.1.1 Address Bus (A[23:0])

The lower 24 bits of the address bus become valid when $\overline{\text{TS}}$ is asserted. A[4:2] indicate the interrupt level during interrupt acknowledge cycles.

17.2.1.2 Address Bus (A[31:24]/PP[15:8])

These multiplexed pins can serve as the most-significant byte of the address bus, or as the most-significant byte of the parallel port. Programming the PAR in the system integration module (SIM) determines the function of each of these eight multiplexed pins. These pins are programmable on a bit-by-bit basis.

- A[31:24]—Pins are configured as address bits by setting corresponding PAR bits; they represent the most-significant address bus bits. As much as 4 Gbytes of memory are available when all of these pins are programmed as address signals.
- PP[15:8]—Pins are configured as parallel port signals by clearing corresponding PAR bits; these represent the most-significant parallel port bits.

17.2.2 Data Bus (D[31:0])

The data bus is bidirectional and non-multiplexed. Data is sampled by the MCF5307 on the rising BCLKO edge. The data bus port width, wait states, and internal termination are initially defined for the boot chip select by D[7:0] during reset. The port width for each chip select and DRAM bank are programmable. The data bus uses a default configuration if none of the chip selects or DRAM bank match the address decode. The default configuration is a 32-bit port with external termination and burst-inhibited transfers. The data bus can transfer byte, word, or longword data widths. All 32 data bus signals are driven during writes, regardless of port width and operand size.

D[7:0] are used during reset initialization as inputs to configure the functions as described in Table 17-3. They are defined in Section 17.5.5, “Data/Configuration Pins (D[7:0]).”

Table 17-3. Data Pin Configuration

Pin	Function	Section
D7	Auto-acknowledge configuration (AA_CONFIG)	Section 17.5.5.2, “D7—Auto Acknowledge Configuration (AA_CONFIG)”
D[6:5]	Port size configuration (PS_CONFIG[1:0])	Section 17.5.5.3, “D[6:5]—Port Size Configuration (PS_CONFIG[1:0])”
D4	Address configuration (ADDR_CONFIG/D4)	Section 17.5.6, “D4—Address Configuration (ADDR_CONFIG)”
D[3:2]	Frequency Control PLL (FREQ[1:0])	Section 17.5.7, “D[3:2]—Frequency Control PLL (FREQ[1:0])
D[1:0]	Divide Control (DIVIDE[1:0])	Section 17.5.8, “D[1:0]—Divide Control PCLK to BCLKO (DIVIDE[1:0])

17.2.3 Read/Write (R/$\overline{W}$)

When the MCF5307 is the bus master, it drives the R/$\overline{W}$ signal to indicate the direction of subsequent data transfers. It is driven high during read bus cycles and driven low during write bus cycles. This signal is an input during an external master access.

17.2.4 Size (SIZ[1:0])

When it is the bus master, the MCF5307 outputs these signals to indicate the requested data transfer size. Table 17-4 shows the definition of the bus request size encodings. When the MCF5307 device is not the bus master, these signals function as inputs.

Note that for misaligned transfers, SIZ[1:0] indicate the size of each transfer. For example, if a longword access occurs at a misaligned offset of 0x1, a byte is transferred first (SIZ[1:0]

= 01), a word is next transferred at offset 0x2 (SIZ[1:0] = 10), then the final byte is transferred at offset 0x4 (SIZ[1:0] = 01).

For aligned transfers larger than the port size, SIZ[1:0] behaves as follows:

- If bursting is used, SIZ[1:0] stays at the size of transfer.
- If bursting is inhibited, SIZ[1:0] first shows the size of the transfer and then shows the port size.

Table 17-4. Bus Cycle Size Encoding

SIZ[1:0]	Port Size
00	Longword
01	Byte
10	Word
11	Line

For burst-inhibited transfers, SIZ[1:0] changes with each $\overline{TS}$ assertion to reflect the next transfer size. For transfers to port sizes smaller than the transfer size, SIZ[1:0] indicates the size of the entire transfer on the first access and the size of the current port transfer on subsequent transfers. For example, for a longword write to an 8-bit port, SIZ[1:0] = 00 for the first byte transfer and 01 for the next three.

17.2.5 Transfer Start ($\overline{TS}$)

The MCF5307 asserts $\overline{TS}$ during the first clock cycle when address and attributes (TM, TT, $\overline{TIP}$, R/$\overline{W}$, and SIZ) are valid. $\overline{TS}$ is negated in the following clock cycle. When the MCF5307 is not the bus master, $\overline{TS}$ is an input.

17.2.6 Address Strobe ($\overline{AS}$)

Address strobe ($\overline{AS}$) is asserted to indicate when the address is stable at the start of a bus cycle. The address and attributes are guaranteed to be valid during the entire period that $\overline{AS}$ is asserted. This signal is asserted and negated on the falling edge of the clock. When the MCF5307 is not the bus master, $\overline{AS}$ is an input.

17.2.7 Transfer Acknowledge ($\overline{TA}$)

When the MCF5307 is bus master, the external system drives this input to terminate the bus transfer. The bus continues to be driven until this synchronous signal is asserted. For write cycles, the processor continues to drive data one clock after $\overline{TA}$ is asserted. During read cycles, the peripheral must continue to drive data until $\overline{TA}$ is recognized.

If all bus cycles support fast termination, $\overline{TA}$ can be tied low. However, note that $\overline{TA}$ cannot be tied low if potential external bus masters are present. The MCF5307 drives $\overline{TA}$ for an

external master access. This condition is indicated by the AM bit in the chip-select mask register (CSMR) being cleared. See Chapter 10, “Chip-Select Module.”

17.2.8 Transfer In Progress ($\overline{\text{TIP}}$/PP7)

The $\overline{\text{TIP}}$/PP7 pin is programmed in the PAR to serve as the transfer-in-progress output or as a parallel port bits. The $\overline{\text{TIP}}$ output is asserted indicating a bus transfer is in progress. It is negated during idle bus cycles if the bus is still granted to the processor. It is three-stated for external master accesses. Note that $\overline{\text{TIP}}$ is held asserted on back-to-back bus cycles.

17.2.9 Transfer Type (TT[1:0]/PP[1:0])

The TT[1:0]/PP[1:0] pins are programmed in the PAR to serve as the transfer type outputs or as two parallel port bits. When the MCF5307 is bus master and TT[1:0] are enabled, these signals are driven as outputs only. If an external master owns the bus and TT[1:0] are enabled, these pins are three-stated by the MCF5307 and can be driven by the external master. Table 17-5 shows the definition of the encodings.

Table 17-5. Bus Cycle Transfer Type Encoding

TT[1:0]	Transfer Type
00	Normal access
01	DMA access
10	Emulator access
11	CPU space or interrupt acknowledge

17.2.10 Transfer Modifier (TM[2:0]/PP[4:2])

The TM[2:0]/PP[4:2] pins are programmed in the PAR to serve as the transfer modifier outputs or as three parallel port bits. These outputs provide supplemental information for each transfer type; see Table 17-6 through Table 17-10.

When the MCF5307 is the bus master and TM[2:0] are enabled, these signals are driven as outputs only. If an external device is bus master and TM[2:0] are enabled, these pins are three-stated by the MCF5307 and can be driven by the external master.

Table 17-6. TM[2:0] Encodings for TT = 00 (Normal Access)

TM[2:0]	Transfer Modifier
000	Cache push access
001	User data access
010	User code access
011–100	Reserved
101	Supervisor data access

Table 17-6. TM[2:0] Encodings for TT = 00 (Normal Access) (Continued)

TM[2:0]	Transfer Modifier
110	Supervisor code access
111	Reserved

As shown in Table 17-7, if the DMA is bus master (TT = 01), TM[2:0] indicate the type of DMA access and provide the DMA acknowledgement information for channels 0 and 1.

NOTE:

When TT= 01, the TM0 encoding is independent from TM[2:1] encoding.

Table 17-7. TM0 Encoding for DMA as Master (TT = 01)

TM0	Transfer Modifier Encoding
0	Single-address access negated
1	Single-address access

Table 17-8. TM[2:1] Encoding for DMA as Master (TT = 01)

TM[2:1]	Transfer Modifier Encoding
00	DMA acknowledges negated
01	DMA acknowledge, channel 0
10	DMA acknowledge, channel 1
11	Reserved

Table 17-9 shows TM[2:0] encodings for emulator mode accesses.

Table 17-9. TM[2:0] Encodings for TT = 10 (Emulator Access)

TM[2:0]	Transfer Modifier
000–100	Reserved
101	Emulator mode data access
110	Emulator mode code access
111	Reserved

The TM signals indicate user or data transfer types during emulation transfers, while for interrupt acknowledge transfers, the TM signals carry the interrupt level being acknowledged; see Table 17-10.

Table 17-10. TM[2:0] Encodings for TT = 11 (Interrupt Level)

TM[2:0]	Transfer Modifier
000	CPU Space
001	Interrupt level 1 acknowledge

Table 17-10. TM[2:0] Encodings for TT = 11 (Interrupt Level) (Continued)

TM[2:0]	Transfer Modifier
010	Interrupt level 2 acknowledge
011	Interrupt level 3 acknowledge
100	Interrupt level 4 acknowledge
101	Interrupt level 5 acknowledge
110	Interrupt level 6 acknowledge
111	Interrupt level 7 acknowledge

17.3 Interrupt Control Signals

The interrupt control signals supply the external interrupt level to the MCF5307 device.

17.3.1 Interrupt Request ($\overline{IRQ1}$/$\overline{IRQ2}$, $\overline{IRQ3}$/$\overline{IRQ6}$, $\overline{IRQ5}$/$\overline{IRQ4}$, and $\overline{IRQ7}$)

The $\overline{IRQ1}$, $\overline{IRQ3}$, $\overline{IRQ5}$, and $\overline{IRQ7}$ signals are the default interrupt request signals ($\overline{IRQn}$). However, by setting the appropriate bit in the interrupt port assignment register (IRQPAR), $\overline{IRQ1}$, $\overline{IRQ3}$, and $\overline{IRQ5}$ can be changed to function as $\overline{IRQ2}$, $\overline{IRQ6}$, and $\overline{IRQ4}$, respectively. See Section 9.2.4, “Interrupt Port Assignment Register (IRQPAR).”

17.4 Bus Arbitration Signals

The bus arbitration signals provide the external bus arbitration control for the MCF5307.

17.4.1 Bus Request ($\overline{BR}$)

The $\overline{BR}$ output indicates to an external arbiter that the processor is requesting to be bus master for one or more bus cycles. $\overline{BR}$ is negated when the MCF5307 begins an access to the external bus with no other internal accesses pending. $\overline{BR}$ remains negated until another internal request occurs.

17.4.2 Bus Grant ($\overline{BG}$)

An external arbiter asserts the $\overline{BG}$ input to indicate that the MCF5307 can take control of the bus on the next rising edge of BCLKO. When the arbiter negates $\overline{BG}$, the MCF5307 will release the bus as soon as the current transfer completes. The external arbiter must not grant the bus to any other master until both $\overline{BD}$ and $\overline{BG}$ are negated.

17.4.3 Bus Driven ($\overline{BD}$)

The MCF5307 asserts $\overline{BD}$ to indicate that it is the current master and is driving the bus. The MCF5307 behaves as follows:

- If the MCF5307 is the bus master but is not using the bus, $\overline{BD}$ is asserted.
- If the MCF5307 loses mastership during a transfer, it completes the last transfer of the access, negates $\overline{BD}$, and three-states all bus signals on the rising edge of BCLKO.
- If the MCF5307 loses bus mastership during an idle clock cycle, it three-states all bus signals on the rising edge of BCLKO.
- $\overline{BD}$ cannot be negated unless $\overline{BG}$ is negated.

17.5 Clock and Reset Signals

The clock and reset signals configure the MCF5307 and provide interface signals to the external system.

17.5.1 Reset In ($\overline{RSTI}$)

Asserting $\overline{RSTI}$ causes the MCF5307 to enter reset exception processing. When $\overline{RSTI}$ is recognized, $\overline{BR}$ and $\overline{BD}$ are negated and the address bus, data bus, TT, SIZ, R/$\overline{W}$, $\overline{AS}$, and $\overline{TS}$ are three-stated. $\overline{RSTO}$ is asserted automatically when $\overline{RSTI}$ is asserted.

17.5.2 Clock Input (CLKIN)

CLKIN is the MCF5307 input clock frequency to the on-board phase-locked-loop (PLL) clock generator. CLKIN is used to internally clock or sequence the MCF5307 internal bus interface at a selected multiple of the input frequency used for internal module logic.

17.5.3 Bus Clock Output (BCLKO)

The internal PLL generates BCLKO and can be programmed to be 1/2, 1/3, or 1/4 of the processor clock frequency. BCLKO should be used as the bus timing reference.

17.5.4 Reset Out ($\overline{RSTO}$)

After $\overline{RSTI}$ is asserted, the PLL temporarily loses its lock, during which time $\overline{RSTO}$ is asserted. When the PLL regains its lock, $\overline{RSTO}$ negates again. This signal can be used to reset external devices.

17.5.5 Data/Configuration Pins (D[7:0])

This section describes data pins, D[7:0], that are read at reset for configuration. Table 17-11 shows pin assignments.

Table 17-11. Data Pin Configuration

Pin	Function
D7	Auto-acknowledge configuration (AA_CONFIG)
D[6:5]	Port size configuration (PS_CONFIG[1:0])
D4	Address configuration (ADDR_CONFIG/D4)
D[3:2]	Frequency Control PLL (FREQ[1:0])
D[1:0]	Divide Control (DIVIDE[1:0])

17.5.5.1 D[7:5Boot Chip-Select ($\overline{CS0}$) Configuration

D[7:5] determine defaults for the global chip select ($\overline{CS0}$), the only chip select valid at reset. These signals correspond to bits in chip-select configuration register 0 (CSCR0).

17.5.5.2 D7—Auto Acknowledge Configuration (AA_CONFIG)

At reset, the enabling and disabling of auto acknowledge for boot $\overline{CS0}$ is determined by the logic level driven on D7 at the rising edge of $\overline{RSTI}$. AA_CONFIG is multiplexed with D7 and sampled only at reset. The D7 logic level is reflected as the reset value of CSCR[AA]. Table 17-12 shows how the D7 logic level corresponds to the auto acknowledge timing for $\overline{CS0}$ at reset. Note that auto acknowledge can be disabled by driving a logic 0 on D7 at reset.

Table 17-12. D7 Selection of $\overline{CS0}$ Automatic Acknowledge

D7 (CSCR0[AA])	Boot $\overline{CS0}$ AA
0	Disabled
1	Enabled with 15 wait states

17.5.5.3 D[6:5]—Port Size Configuration (PS_CONFIG[1:0])

The default port size value of the boot $\overline{CS0}$ is determined by the logic levels driven on D[6:5] at the rising edge of $\overline{RSTI}$, which are reflected as the reset value of CSCR[PS]. Table 17-13 shows how the logic levels of D[6:5] correspond to the $\overline{CS0}$ port size at reset.

Table 17-13. D6 and D5 Selection of $\overline{CS0}$ Port Size

D[6:5] (CSCR0[PS])	Boot $\overline{CS0}$ Port Size
00	32-bit port
01	8-bit port
1x	16-bit port

17.5.6 D4—Address Configuration (ADDR_CONFIG)

The address configuration signal (ADDR_CONFIG) programs the PAR of the parallel I/O port to be either parallel I/O or to be the upper address bus bits along with various attribute and control signals at reset to give the user the option to access a broader addressing range

of memory if desired. ADDR_CONFIG is multiplexed with D4 and its configuration is sampled at reset as shown in Table 17-14.

Table 17-14. D4/ADDR_CONFIG, Address Pin Assignment

D4/ADDR_CONFIG	PAR Configuration at Reset
0	PP[15:0], defaulted to inputs upon reset
1	A[31:24]/$\overline{\text{TIP}}$/$\overline{\text{DREQ}}$[1:0]/TM[2:0]/TT[1:0]

17.5.7 D[3:2]—Frequency Control PLL (FREQ[1:0])

The frequency control PLL input bus (FREQ[1:0]) indicates the CLKIN frequency range. These signals are multiplexed with D[3:2] and are sampled during the assertion of $\overline{\text{RESET}}$. These signals indicate the operating frequency range to the PLL, as shown in Table 17-15. Note that these signals do not affect the PLL frequency but are required to set up the analog PLL.

Table 17-15. CLKIN Frequency

FREQ[1:0]/D[3:2]	CLKIN Frequency (MHz)
00	16.6–27.999
01	28–38.999
10	39–45
11	Reserved

17.5.8 D[1:0]—Divide Control PCLK to BCLKO (DIVIDE[1:0])

This 2-bit input bus indicates the BCLKO/PSTCLK ratio. These signals are sampled during the assertion of $\overline{\text{RESET}}$ and indicate the ratios shown in Table 17-16.

Table 17-16. BCLKO/PSTCLK Divide Ratios

DIVIDE[1:0]/D[1:0]	Ratio of BCLKO/PSTCLK
00	1/4
01	Reserved
10	1/2
11	1/3

17.6 Chip-Select Module Signals

The MCF5307 device provides eight programmable chip-select signals that can directly interface with SRAM, EPROM, EEPROM, and peripherals. These signals are asserted and negated on the falling edge of the clock.

17.6.1 Chip-Select ($\overline{CS}$[7:0])

Each chip select can be programmed for a base address location and for masking addresses, port size and burst-capability indication, wait-state generation, and internal/external termination.

Reset clears all chip select programming; $\overline{CS0}$ is the only chip select initialized out of reset. $\overline{CS0}$ is also unique because it can function at reset as a global chip select that allows boot ROM to be selected at any defined address space. Port size and termination (internal vs. external) for boot $\overline{CS0}$ are configured by the levels on D[7:5] on the rising edge of $\overline{RSTI}$, as described in Section 17.5.5.1, “D[7:5Boot Chip-Select (CS0) Configuration.”

The chip-select implementation is described in Chapter 10, “Chip-Select Module.”

17.6.2 Byte Enables/Byte Write Enables ($\overline{BE}$[3:0]/$\overline{BWE}$[3:0])

The four byte enables are multiplexed with the MCF5307 byte-write-enable signals. Each pin can be individually programmed through the chip-select control registers (CSCRs). For each chip select, assertion of byte enables for reads and byte-write enables for write cycles can be programmed. Alternatively, users can program byte-write enables to assert on writes and no byte enable assertion for read transfers.

17.6.3 Output Enable ($\overline{OE}$)

The output enable ($\overline{OE}$) signal is sent to the interfacing memory and/or peripheral to enable a read transfer. $\overline{OE}$ is asserted only when a chip select matches the current address decode.

17.7 DRAM Controller Signals

The DRAM signals in the following sections interface to external DRAM. DRAM with widths of 8, 16, and 32 bits are supported and can access as much as 512 Mbytes of DRAM.

17.7.1 Row Address Strobes ($\overline{RAS}$[1:0])

The row address strobes ($\overline{RAS}$[1:0]) interface to $\overline{RAS}$ inputs on industry-standard ADRAMs. When SDRAMs are used, these signals interface to the chip-select lines of the SDRAMs within a memory block. Thus, there is one $\overline{RAS}$ line for each memory block.

17.7.2 Column Address Strobes ($\overline{CAS}$[3:0])

The column address strobes ($\overline{CAS}$[3:0]) interface to $\overline{CAS}$ inputs on industry-standard DRAMs. These provide $\overline{CAS}$ for a given ADRAM block. When SDRAMs are used, $\overline{CAS}$ signals control the byte enables for standard SDRAMs (referred to as DQM*x*). $\overline{CAS3}$ accesses the LSB and $\overline{CAS0}$ accesses the MSB of data.

17.7.3 DRAM Write ($\overline{\text{DRAMW}}$)

The DRAM write signal ($\overline{\text{DRAMW}}$) is asserted to signify that a DRAM write cycle is underway. A read bus cycle is indicated by the negation of $\overline{\text{DRAMW}}$.

17.7.4 Synchronous DRAM Column Address Strobe ($\overline{\text{SCAS}}$)

The synchronous DRAM column address strobe ($\overline{\text{SCAS}}$) is registered during synchronous mode to route directly to the $\overline{\text{SCAS}}$ signal of SDRAMs.

17.7.5 Synchronous DRAM Row Address Strobe ($\overline{\text{SRAS}}$)

The synchronous DRAM row address strobe output ($\overline{\text{SRAS}}$) is registered during synchronous mode to route directly to the $\overline{\text{SRAS}}$ signal of external SDRAMs.

17.7.6 Synchronous DRAM Clock Enable (SCKE)

The synchronous DRAM clock enable output (SCKE) is registered during synchronous mode to route directly to the SCKE signal of external SDRAMs. This signal provides the clock enable to the SDRAM.

17.7.7 Synchronous Edge Select (EDGESEL)

The synchronous edge select input (EDGESEL) helps select additional output hold times for signals that interface to external SDRAMs. It provides the following three modes of operation for SDRAM control signals:

- When EDGESEL is tied high, SDRAM control signals change on the rising edge of BCLKO.
- When EDGESEL is tied low, SDRAM control signals change on the falling edge of BCLKO.
- When EDGESEL is tied to the external clock (normally buffered BCLKO), which drives the SDRAM and other devices, SDRAM signals are generated within the MCF5307 make a transition on the rising edge of the SDRAM clock. See Figure 11-14 on page 11-19. This loop-back configuration provides additional output hold time for MCF5307 interface signals provided to the SDRAM. In this case, the SDRAM clock operates at the BCLKO frequency, with a possible slight phase delay.

17.8 DMA Controller Module Signals

The DMA controller module uses the signals in the following subsections to provide external request for either a source or destination.

17.8.1 DMA Request ($\overline{\text{DREQ}}$[1:0]/PP[6:5])

The DMA request pins ($\overline{\text{DREQ}}$[1:0]/PP[6:5]) can serve as the DMA request inputs or as two bits of the parallel port, as determined by individually programmable bits in the PAR.

These inputs are asserted by a peripheral device to request an operand transfer between that peripheral and memory by either channel 0 or 1 of the on-chip DMA.

Note that DMA acknowledge indication is displayed on TM[2:0], during DMA transfers of channel 0 and 1.

17.9 Serial Module Signals

The signals in the following sections are used to transfer serial data between the two UART modules and external peripherals.

17.9.1 Transmitter Serial Data Output (TxD)

TxD is held high (mark condition) when the transmitter is disabled, idle, or operating in the local loop-back mode. Data is shifted out least-significant bit (lsb) first on TxD on the falling edge of the clock source.

17.9.2 Receiver Serial Data Input (RxD)

Data received on RxD is sampled on the rising edge of the clock source, with the lsb received first.

17.9.3 Clear to Send ($\overline{\text{CTS}}$)

This input can generate an interrupt on a change of state.

17.9.4 Request to Send ($\overline{\text{RTS}}$)

This output can be programmed to be negated or asserted automatically by either the receiver or the transmitter. When connected to a transmitter's $\overline{\text{CTS}}$, $\overline{\text{RTS}}$ can control serial data flow.

17.10 Timer Module Signals

The signals in the following sections are external interfaces to the two general-purpose MCF5307 timers. These 16-bit timers can capture timer values, trigger external events or internal interrupts, or count external events.

17.10.1 Timer Inputs (TIN[1:0])

TIN[1:0] can be programmed as clocks that cause events in the counter and prescalers. They can also cause captures on the rising edge, falling edge, or both edges.

17.10.2 Timer Outputs (TOUT1, TOUT0)

The programmable timer outputs (TOUT1 and TOUT0) pulse or toggle on various timer events.

17.11 Parallel I/O Port (PP[15:0])

This 16-bit bus is dedicated for general-purpose I/O. The parallel port is multiplexed with the A[31:24], TT[1:0], TM[2:0], $\overline{\text{TIP}}$, and $\overline{\text{DREQ}}$[1:0]. These 16 bits are programmed for functionality with the PAR in the SIM.

The system designer controls the reset value of this register by driving D4 with a 1 or 0 on the rising edge of $\overline{\text{RSTI}}$ (reset input to MCF5307 device). At reset, the system is configured as PP[15:0] if D4 is 0; otherwise alternate pin functions selected by PAR = 1 are used. Motorola recommends that D4 be driven during reset to a logic level.

17.12 I^2C Module Signals

The I^2C module acts as a two-wire, bidirectional serial interface between the MCF5307 and peripherals with an I^2C interface (such as LED controller, A-to-D converter, or D-to-A converter). Devices connected to the I^2C must have open-drain or open-collector outputs.

17.12.1 I^2C Serial Clock (SCL)

The bidirectional, open-drain I^2C serial clock signal (SCL) is the clock signal for I^2C module operation. The I^2C module controls this signal when the bus is in master mode; all I^2C devices drive this signal to synchronize I^2C timing.

17.12.2 I^2C Serial Data (SDA)

The bidirectional, open-drain I^2C serial data signal (SDA) is the data input/output for the serial I^2C interface.

17.13 Debug and Test Signals

The signals in this section interface with external I/O to provide processor status signals.

17.13.1 Test Mode (MTMOD[3:0])

The test mode signals choose between multiplexed debug module and JTAG signals. If MTMOD0 is low, the part is in normal and background debug mode (BDM); if it is high, it is in normal and JTAG mode. All other MTMOD values are reserved; MTMOD[3:1] should be tied to ground and MTMOD[3:0] should not be changed while $\overline{\text{RSTI}}$ is negated.

17.13.2 High Impedance ($\overline{\text{HIZ}}$)

The assertion of $\overline{\text{HIZ}}$ forces all output drivers to high-impedance state. The timing on $\overline{\text{HIZ}}$ is independent of the clock. Note that $\overline{\text{HIZ}}$ does not override the JTAG operation; TDO/DSO can be forced to high impedance by asserting $\overline{\text{TRST}}$.

17.13.3 Processor Clock Output (PSTCLK)

The internal PLL generates this output signal, and is the processor clock output that is used as the timing reference for the debug bus timing (DDATA[3:0] and PST[3:0]). PSTCLK is at the same frequency as the core processor and cache memory. The frequency is 2x the CLKIN.

17.13.4 Debug Data (DDATA[3:0])

The debug data signals (DDATA[3:0]) display captured processor data and breakpoint status. See Chapter 5, “Debug Support,” for additional information on this bus.

17.13.5 Processor Status (PST[3:0])

The processor status pins indicate the MCF5307 processor status. During debug mode, the timing is synchronous with the processor clock (PSTCLK) and the status is not related to the current bus transfer. Table 2-11 shows the encodings of these signals.

Table 17-17. Processor Status Signal Encodings

PST[3:0]		Definition
Hex	Binary	
0x0	0000	Continue execution
0x1	0001	Begin execution of an instruction
0x2	0010	Reserved
0x3	0011	Entry into user-mode
0x4	0100	Begin execution of PULSE and WDDATA instructions
0x5	0101	Begin execution of taken branch or Synch_PC[1]
0x6	0110	Reserved
0x7	0111	Begin execution of RTE instruction
0x8	1000	Begin 1-byte data transfer on DDATA
0x9	1001	Begin 2-byte data transfer on DDATA
0xA	1010	Begin 3-byte data transfer on DDATA
0xB	1011	Begin 4-byte data transfer on DDATA
0xC	1100	Exception processing[2]
0xD	1101	Emulator mode entry exception processing[2]
0xE	1110	Processor is stopped, waiting for interrupt[2]
0xF	1111	Processor is halted[2]

1 Rev. B enhancement.

2 These encodings are asserted for multiple cycles.

17.14 Debug Module/JTAG Signals

The MCF5307 complies with the IEEE 1149.1a JTAG testing standard. JTAG test pins are multiplexed with background debug pins. Except for TCK, these signals are selected by the value of MTMOD0. If MTMOD0 is high, JTAG signals are chosen; if it is low, debug module signals are chosen. MTMOD0 should be changed only while $\overline{\text{RSTI}}$ is asserted.

17.14.1 Test Reset/Development Serial Clock ($\overline{\text{TRST}}$/DSCLK)

If MTMOD0 is high, $\overline{\text{TRST}}$ is selected. $\overline{\text{TRST}}$ asynchronously resets the internal JTAG controller to the test logic reset state, causing the JTAG instruction register to choose the bypass instruction. When this occurs, JTAG logic is benign and does not interfere with normal MCF5307 functionality.

Although $\overline{\text{TRST}}$ is asynchronous, Motorola recommends that it makes an asserted-to-negated transition only while TMS is held high. $\overline{\text{TRST}}$ has an internal pull-up resistor so if it is not driven low, it defaults to a logic level of 1. If $\overline{\text{TRST}}$ is not used, it can be tied to ground or, if TCK is clocked, to V_{DD}. Tying $\overline{\text{TRST}}$ to ground places the JTAG

controller in test logic reset state immediately. Tying it to V_{DD} causes the JTAG controller (if TMS is a logic level of 1) to eventually enter test logic reset state after 5 TCK clocks.

If MTMOD0 is low, DSCLK is selected. DSCLK is the development serial clock for the serial interface to the debug module. The maximum DSCLK frequency is 1/5 CLKIN. See Chapter 5, “Debug Support.”

17.14.2 Test Mode Select/Breakpoint (TMS/$\overline{\text{BKPT}}$)

If MTMOD0 is high, TMS is selected. The TMS input provides information to determine the JTAG test operation mode. The state of TMS and the internal 16-state JTAG controller state machine at the rising edge of TCK determine whether the JTAG controller holds its current state or advances to the next state. This directly controls whether JTAG data or instruction operations occur. TMS has an internal pull-up resistor so that if it is not driven low, it defaults to a logic level of 1. But if TMS is not used, it should be tied to V_{DD}.

If MTMOD0 is low, $\overline{\text{BKPT}}$ is selected. $\overline{\text{BKPT}}$ signals a hardware breakpoint to the processor in debug mode. See Chapter 5, “Debug Support.”

17.14.3 Test Data Input/Development Serial Input (TDI/DSI)

If MTMOD0 is high, TDI is selected. TDI provides the serial data port for loading the various JTAG boundary scan, bypass, and instruction registers. Shifting in data depends on the state of the JTAG controller state machine and the instruction in the instruction register. Shifts occur on the TCK rising edge. TDI has an internal pull-up resistor, so when not driven low it defaults to high. But if TDI is not used, it should be tied to V_{DD}.

If MTMOD0 is low, DSI is selected. DSI provides the single-bit communication for debug module commands. See Chapter 5, “Debug Support.”

17.14.4 Test Data Output/Development Serial Output (TDO/DSO)

If MTMOD0 is high, TDO is selected. The TDO output provides the serial data port for outputting data from JTAG logic. Shifting out data depends on the JTAG controller state machine and the instruction in the instruction register. Data shifting occurs on the falling edge of TCK. When TDO is not outputting test data, it is three-stated. TDO can be three-stated to allow bused or parallel connections to other devices having JTAG.

If MTMOD0 is low, DSO is selected. DSO provides single-bit communication for debug module responses. See Chapter 5, “Debug Support.”

17.14.5 Test Clock (TCK)

TCK is the dedicated JTAG test logic clock independent of the MCF5307 processor clock. Various JTAG operations occur on the rising or falling edge of TCK. Holding TCK high or low for an indefinite period does not cause JTAG test logic to lose state information. If TCK is not used, it must be tied to ground.