Chapter 13
Timer Module

This chapter describes the configuration and operation of the two general-purpose timer modules (timer 0 and timer 1). It includes programming examples.

13.1 Overview

The timer module incorporates two independent, general-purpose 16-bit timers, timer 0 and timer 1. The output of an 8-bit prescaler clocks each timer. There are two sets of registers, one for each timer. The timers can operate from the system bus clock (BCLKO) or from an external clocking source using one of the TIN signals. If BCLKO is selected, it can be divided by 16 or 1.

Figure 13-1 is a block diagram of one of the two identical ti5mer modules.

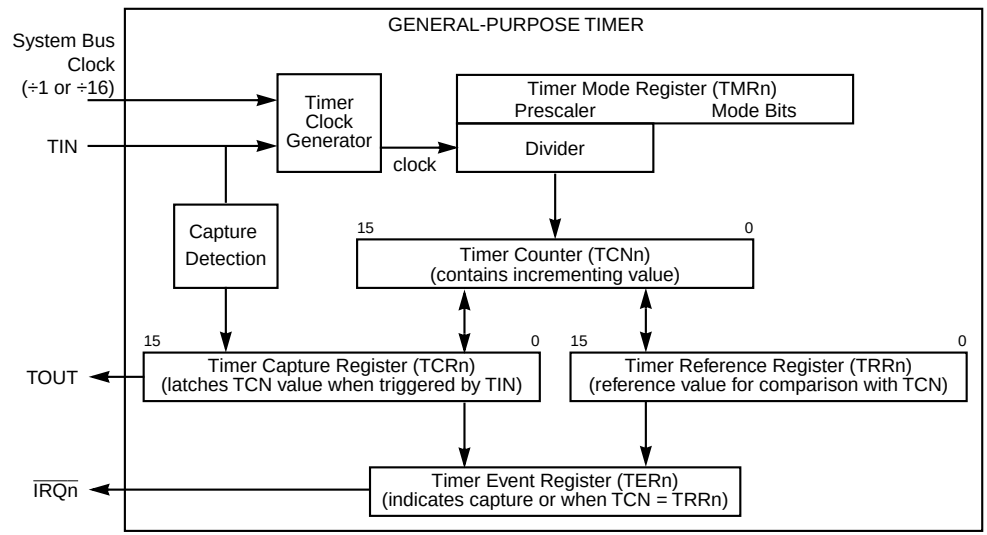

Figure 13-1. Timer Block Diagram

13.1.1 Key Features

Each general-purpose 16-bit timer unit has the following features:

- Maximum period of 5.96 seconds at 45 MHz
- 27-nS resolution at 45 MHz
- Programmable sources for the clock input, including external clock
- Input-capture capability with programmable trigger edge on input pin
- Output-compare with programmable mode for the output pin
- Free run and restart modes
- Maskable interrupts on input capture or reference-compare

13.2 General-Purpose Timer Units

The general-purpose timer units provide the following features:

- Each timer can be programmed to count and compare to a reference value stored in a register or capture the timer value at an edge detected on TIN.
- System bus clock can be divided by 16 or 1. This clock is input to the prescaler.
- TIN is fed directly into the 8-bit prescaler. The maximum value of TIN is 1/5 of CLKIN, as described in Chapter 20, “Electrical Specifications.”
- The 8-bit prescaler clock divides the clocking source and is user-programmable from 1 to 256.
- Programmed events generate interrupts.
- The timer output signal (TOUT) can be configured to toggle or pulse on an event.

13.3 General-Purpose Timer Programming Model

The following features are programmable through the timer registers, shown in Table 13-1:

- Prescaler—The prescaler clock input is selected from BCLKO (divided by 1 or 16) or from the corresponding timer input, TIN. TIN is synchronized to BCLKO. The synchronization delay is between two and three BCLKO clocks. The corresponding TMR*n*[ICLK] selects the clock input source. A programmable prescaler divides the clock input by values from 1 to 256. The prescaler is an input to the 16-bit counter.
- Capture mode—Each timer has a 16-bit timer capture register (TCR0 and TCR1) that latches the counter value when the corresponding input capture edge detector senses a defined TIN transition. The capture edge bits (TMR*n*[CE]) select the type of transition that triggers the capture, sets the timer event register capture event bit, TER*n*[CAP], and issues a maskable interrupt.

- Reference compare—A timer can be configured to count up to a reference value, at which point TER*n*[REF] is set. If TMR*n*[ORI] is one, an interrupt is issued. If the free run/restart bit TMR*n*[FRR] is set, a new count starts. If it is clear, the timer keeps running.
- Output mode—When a timer reaches the reference value selected by TMR*n*[OM], it can send an output signal on TOUT*n*. TOUT*n* can be an active-low pulse or a toggle of the current output under program control.

NOTE:

Although external devices cannot access MCF5307 on-chip memories or MBAR, they can access timer module registers.

The timer module registers, shown in Table 13-1, can be modified at any time.

Table 13-1. General-Purpose Timer Module Memory Map

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x140	Timer 0 mode register (TMR0) [p. 13-3]		Reserved	
0x144	Timer 0 reference register (TRR0) [p. 13-4]		Reserved	
0x148	Timer 0 capture register (TCR0) [p. 13-4]		Reserved	
0x14C	Timer 0 counter (TCN0) [p. 13-5]		Reserved	
0x150	Reserved	Timer 0 event register (TER0) [p. 13-5]	Reserved	
0x180	Timer 1 mode register (TMR1) [p. 13-3]		Reserved	
0x184	Timer 1 reference register (TRR1) [p. 13-4]		Reserved	
0x188	Timer 1 capture register (TCR1) [p. 13-4]		Reserved	
0x18C	Timer 1 counter (TCN1) [p. 13-5]		Reserved	
0x190	Reserved	Timer 1 event register (TER1) [p. 13-5]	Reserved	

13.3.1 Timer Mode Registers (TMR0/TMR1)

Timer mode registers (TMR0/TMR1), Figure 13-2, program the prescaler and various timer modes.

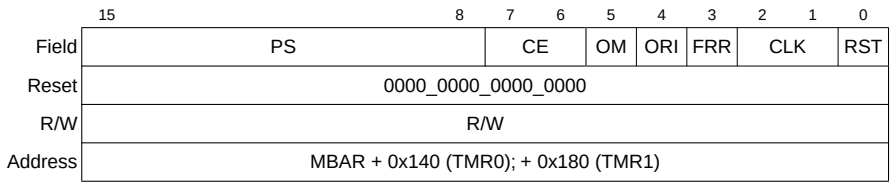

Figure 13-2. Timer Mode Registers (TMR0/TMR1)

Table 13-2 describes TMR*n* fields.

Table 13-2. TMR*n* Field Descriptions

Bits	Name	Description
15–8	PS	Prescaler value. The prescaler is programmed to divide the clock input (BCLKO/(16 or 1) or clock on TIN) by values from 1 (PS = 0000_0000) to 256 (PS = 1111_1111).
7–6	CE	Capture edge and enable interrupt 00 Disable interrupt on capture event 01 Capture on rising edge only and enable interrupt on capture event 10 Capture on falling edge only and enable interrupt on capture event 11 Capture on any edge and enable interrupt on capture event
5	OM	Output mode 0 Active-low pulse for one BCLKO cycle (22 nS at 45 MHz, 33 nS at 30 MHz, 44 nS at 22.5 MHz). 1 Toggle output.
4	ORI	Output reference interrupt enable. If ORI is set when TERn[REF] = 1, an interrupt occurs. 0 Disable interrupt for reference reached (does not affect interrupt on capture function). 1 Enable interrupt upon reaching the reference value.
3	FRR	Free run/restart 0 Free run. Timer count continues to increment after reaching the reference value. 1 Restart. Timer count is reset immediately after reaching the reference value.
2–1	CLK	Input clock source for the timer 00 Stop count 01 System bus clock divided by 1 10 System bus clock divided by 16. Note that this clock source is not synchronized to the timer; thus successive time-outs may vary slightly. 11 TIN pin (falling edge)
0	RST	Reset timer. Performs a software timer reset similar to an external reset, although other register values can still be written while RST = 0. A transition of RST from 1 to 0 resets register values. The timer counter is not clocked unless the timer is enabled. 0 Reset timer (software reset) 1 Enable timer

13.3.2 Timer Reference Registers (TRR0/TRR1)

Each timer reference register (TRR0/TRR1), Figure 13-3, contains the reference value compared with the respective free-running timer counter (TCN0/TCN1) as part of the output-compare function. The reference value is not matched until TCN*n* equals TRR*n*.

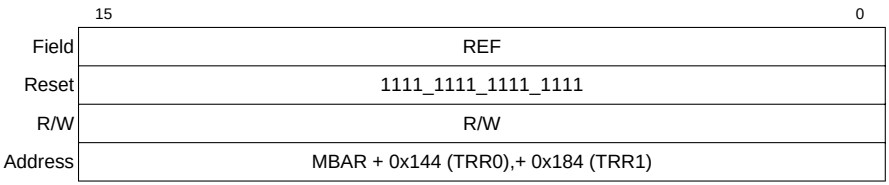

Figure 13-3. Timer Reference Registers (TRR0/TRR1)

13.3.3 Timer Capture Registers (TCR0/TCR1)

Each timer capture register (TCR0/TCR1), Figure 13-4, latches the corresponding TCN*n* value during a capture operation when an edge occurs on TIN, as programmed in TMR*n*.

BCLKO is assumed to be the clock source. TIN cannot simultaneously function as a clocking source and as an input capture pin.

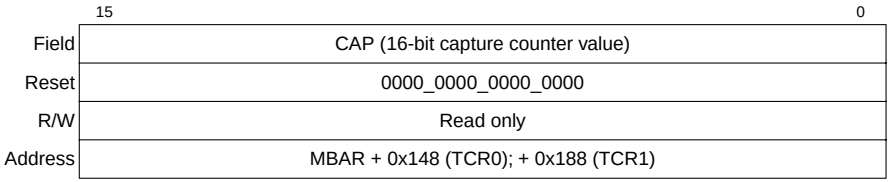

Figure 13-4. Timer Capture Register (TCR0/TCR1)

13.3.4 Timer Counters (TCN0/TCN1)

The current value of the 16-bit, incrementing timer counters (TCN0/TCN1), Figure 13-5, can be read anytime without affecting counting. Writing to TCN*n* clears it. The timer counter decrements on the clock source rising edge (BCLKO ÷ 1, BCLKO ÷ 16, or TIN).

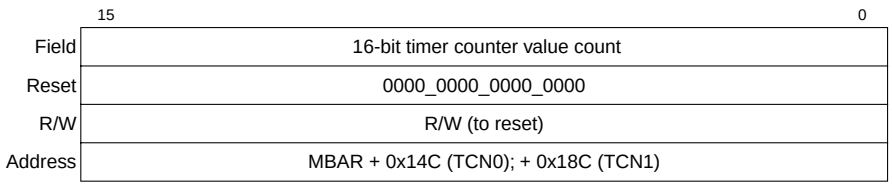

Figure 13-5. Timer Counters (TCN0/TCN1)

13.3.5 Timer Event Registers (TER0/TER1)

Each timer event register (TER0/TER1), Figure 13-6, reports capture or reference events events the timer recognizes by setting TER*n*[CAP] or TER*n*[REF], which it does regardless of the corresponding interrupt-enable bit values, TMR*n*[ORI,CE].

Writing a 1 to either REF or CAP clears it (writing a 0 does not affect bit value); both bits can be cleared at the same time. REF and CAP must be cleared early in the exception handler, before the timer negates the $\overline{\text{IRQ}n}$ to the interrupt controller.

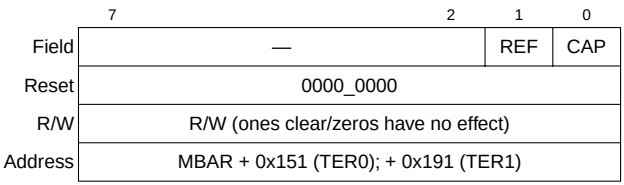

Figure 13-6. Timer Event Registers (TER0/TER1)

Table 13-3 describes TER*n* fields.

Table 13-3. TER*n* Field Descriptions

Bits	Name	Description
7–2	—	Reserved
1	REF	Output reference event. The counter has reached the TRRn value. Setting TMRn[ORI] enables the interrupt request caused by this event. Writing a one to REF clears the event condition.
0	CAP	Capture event. The counter value has been latched into TCRn. Setting TMRn[CE] enables the interrupt request caused by this event. Writing a 1 to CAP clears the event condition.

13.4 Code Example

The following code provides an example of how to initialize timer 0 and how to use the timer for counting time-out periods.

```
MBARx EQU 0x10000 ;Defines the module base address at 0x10000
TMR0 EQU MBARx+0x140;Timer 0 register
TMR1 EQU MBARx+0x180 ;Timer 1 register
TRR0 EQU MBARx+0x144 ;Timer 0 reference register
TRR1 EQU MBARx+0x184 ;Timer 1 reference register
TCR0 EQU MBARx+0x148 ;Timer 0 capture register
TCR1 EQU MBARx+0x188 ;Timer 1 capture register
TCN0 EQU MBARx+0x14C ;Timer 0 counter
TCN1 EQU MBARx+0x18C ;Timer 1 counter
TER0 EQU MBARx+0x151 ;Timer 0 event register
TER1 EQU MBARx+0x191 ;Timer 1 event register

* TMR0 is defined as: *
*[PS]= 0xFF, divide clock by 256
*[CE] = 00disable interrupt
*[OM] = 0 output=active-low pulse
*[ORI] = 0, disable ref.interrupt
*[FRR] = 1, restart mode enabled
*[CLK] = 10, BCLKO/16
*[RST] = 0, timer 0 disabled

    move.w #0xFF0C,D0
    move.w D0,TMR0

    move.w #0x0000,D0;writing to the timer counter with any
    move.w DO,TCN0 ;value resets it to zero

    move.w #AFAF,DO ;set the timer 0 reference to be
    move.w #D0,TRR0 ;defined as 0xAFAF
```

The simple example below uses 0 to count time-out loops. A time-out occurs when the reference value, 0xAFAF, is reached.

```
timer0_ex
    clr.l DO
    clr.l D1
    clt.l D2

    move.w #0x0000,D0
    move,w D0,TCN0;reset the counter to 0x0000

    move.b #0x03,D0 ;writing ones to TER0[REF,CAP]
    move.b D0,TER0 ;clears the event flags
```

```
    move.w TMR0,D0;save the contents of TMR0 while setting
    bset #0,D0 ;the 0 bit. This enables timer 0 and starts counting
    move.w D0, TMR0 ;load the value back into the register, setting TMR0[RST]

T0_LOOP

    move.b TER0,D1 ;load TER0 and see if
    btst #1,D1 ;TER0[REF] has been set
    beq T0_LOOP

    addi.l #1,D2;Increment D2
    cmp.l #5,D2;Did D2 reach 5? (i.e. timer ref has timed)
    beq T0_FINISH;If so, end timer0 example. Otherwise jump back.

    move.b #0x02,D0 ;writing one to TER0[REF] clears the event flag
    move.b D0,TER0
    jmp T0_LOOP

T0_FINISH
    HALT;End processing. Example is finished
```

13.5 Calculating Time-Out Values

The formula below determines time-out periods for various reference values:

> Time-out period = (1/clock frequency) x (1 or 16) x (TMR*n*[PS] + 1) x (TRR*n*[REF])

When calculating time-out periods, add 1 to the prescaler to simplify calculating, because TMR*n*[PS] = 0x00 yields a prescaler of 1 and TMR*n*[PS] = 0xFF yields a prescaler of 256. For example, if a 45-MHz timer clock is divided by 16, TMR*n*[PS] = 0x7F, and the timer is referenced at 0xABCD (43,981 decimal), the time-out period is as follows:

> Time-out period = (1/45) x (16) x (127 + 1) x (43,981) = 1.67 S

The time-out values in Table 13-5 represent the time it takes the counter value in TCN*n* value to go from 0x0000 to the default reference value, TRR*n*[REF] = 0xFFFF. Time-out values shown for BCLKO are divided by 1 and by 16 (TMR*n*[CLK] is 01 or 10, respectively).

Any clock source (BCLKO ÷ 1, BCLKO ÷ 16, or TIN) can be prescaled using TMR*n*[PS].

The BCLKO frequency depends on the prescaler value (TMR*n*[PS]) and on the PLL clock setting, as described inChapter 7, “Phase-Locked Loop (PLL).”

Table 13-5. Calculated Time-out Values (90-MHz Processor Clock)

TMR[PS]		TMR[CLK] = 10 (System Bus Clock/16)			TMR[CLK] = 01 (System Bus Clock/1)		
Decimal	Hex	45 MHz	30 MHz	22.5 MHz	45 MHz	30 MHz	22.5 MHz
0	0	0.0233	0.03495	0.0466	0.00146	0.00218	0.00291
1	1	0.0466	0.06991	0.09321	0.00291	0.00437	0.00583
2	2	0.06991	0.10486	0.13981	0.00437	0.00655	0.00874
3	3	0.09321	0.13981	0.18641	0.00583	0.00874	0.01165
4	4	0.11651	0.17476	0.23302	0.00728	0.01092	0.01456
5	5	0.13981	0.20972	0.27962	0.00874	0.01311	0.01748

Table 13-5. Calculated Time-out Values (90-MHz Processor Clock) (Continued)

TMR[PS]		TMR[CLK] = 10 (System Bus Clock/16)			TMR[CLK] = 01 (System Bus Clock/1)		
Decimal	Hex	45 MHz	30 MHz	22.5 MHz	45 MHz	30 MHz	22.5 MHz
6	6	0.16311	0.24467	0.32622	0.01019	0.01529	0.02039
7	7	0.18641	0.27962	0.37283	0.01165	0.01748	0.0233
8	8	0.20972	0.31457	0.41943	0.01311	0.01966	0.02621
9	9	0.23302	0.34953	0.46603	0.01456	0.02185	0.02913
10	0A	0.25632	0.38448	0.51264	0.01602	0.02403	0.03204
11	0B	0.27962	0.41943	0.55924	0.01748	0.02621	0.03495
12	0C	0.30292	0.45438	0.60584	0.01893	0.0284	0.03787
13	0D	0.32622	0.48934	0.65245	0.02039	0.03058	0.04078
14	0E	0.34953	0.52429	0.69905	0.02185	0.03277	0.04369
15	0F	0.37283	0.55924	0.74565	0.0233	0.03495	0.0466
16	10	0.39613	0.59419	0.79226	0.02476	0.03714	0.04952
17	11	0.41943	0.62915	0.83886	0.02621	0.03932	0.05243
18	12	0.44273	0.6641	0.88546	0.02767	0.04151	0.05534
19	13	0.46603	0.69905	0.93207	0.02913	0.04369	0.05825
20	14	0.48934	0.734	0.97867	0.03058	0.04588	0.06117
21	15	0.51264	0.76896	1.02527	0.03204	0.04806	0.06408
22	16	0.53594	0.80391	1.07188	0.0335	0.05024	0.06699
23	17	0.55924	0.83886	1.11848	0.03495	0.05243	0.06991
24	18	0.58254	0.87381	1.16508	0.03641	0.05461	0.07282
25	19	0.60584	0.90877	1.21169	0.03787	0.0568	0.07573
26	1A	0.62915	0.94372	1.25829	0.03932	0.05898	0.07864
27	1B	0.65245	0.97867	1.30489	0.04078	0.06117	0.08156
28	1C	0.67575	1.01362	1.3515	0.04223	0.06335	0.08447
29	1D	0.69905	1.04858	1.3981	0.04369	0.06554	0.08738
30	1E	0.72235	1.08353	1.4447	0.04515	0.06772	0.09029
31	1F	0.74565	1.11848	1.49131	0.0466	0.06991	0.09321
32	20	0.76896	1.15343	1.53791	0.04806	0.07209	0.09612
33	21	0.79226	1.18839	1.58451	0.04952	0.07427	0.09903
34	22	0.81556	1.22334	1.63112	0.05097	0.07646	0.10194
35	23	0.83886	1.25829	1.67772	0.05243	0.07864	0.10486
36	24	0.86216	1.29324	1.72432	0.05389	0.08083	0.10777
37	25	0.88546	1.3282	1.77093	0.05534	0.08301	0.11068
38	26	0.90877	1.36315	1.81753	0.0568	0.0852	0.1136
39	27	0.93207	1.3981	1.86414	0.05825	0.08738	0.11651
40	28	0.95537	1.43305	1.91074	0.05971	0.08957	0.11942
41	29	0.97867	1.46801	1.95734	0.06117	0.09175	0.12233
42	2A	1.00197	1.50296	2.00395	0.06262	0.09393	0.12525
43	2B	1.02527	1.53791	2.05055	0.06408	0.09612	0.12816
44	2C	1.04858	1.57286	2.09715	0.06554	0.0983	0.13107
45	2D	1.07188	1.60782	2.14376	0.06699	0.10049	0.13398

Table 13-5. Calculated Time-out Values (90-MHz Processor Clock) (Continued)

TMR[PS]		TMR[CLK] = 10 (System Bus Clock/16)			TMR[CLK] = 01 (System Bus Clock/1)		
Decimal	Hex	45 MHz	30 MHz	22.5 MHz	45 MHz	30 MHz	22.5 MHz
46	2E	1.09518	1.64277	2.19036	0.06845	0.10267	0.1369
47	2F	1.11848	1.67772	2.23696	0.06991	0.10486	0.13981
48	30	1.14178	1.71267	2.28357	0.07136	0.10704	0.14272
49	31	1.16508	1.74763	2.33017	0.07282	0.10923	0.14564
50	32	1.18839	1.78258	2.37677	0.07427	0.11141	0.14855
51	33	1.21169	1.81753	2.42338	0.07573	0.1136	0.15146
52	34	1.23499	1.85248	2.46998	0.07719	0.11578	0.15437
53	35	1.25829	1.88744	2.51658	0.07864	0.11796	0.15729
54	36	1.28159	1.92239	2.56319	0.0801	0.12015	0.1602
55	37	1.30489	1.95734	2.60979	0.08156	0.12233	0.16311
56	38	1.3282	1.99229	2.65639	0.08301	0.12452	0.16602
57	39	1.3515	2.02725	2.703	0.08447	0.1267	0.16894
58	3A	1.3748	2.0622	2.7496	0.08592	0.12889	0.17185
59	3B	1.3981	2.09715	2.7962	0.08738	0.13107	0.17476
60	3C	1.4214	2.1321	2.84281	0.08884	0.13326	0.17768
61	3D	1.4447	2.16706	2.88941	0.09029	0.13544	0.18059
62	3E	1.46801	2.20201	2.93601	0.09175	0.13763	0.1835
63	3F	1.49131	2.23696	2.98262	0.09321	0.13981	0.18641
64	40	1.51461	2.27191	3.02922	0.09466	0.14199	0.18933
65	41	1.53791	2.30687	3.07582	0.09612	0.14418	0.19224
66	42	1.56121	2.34182	3.12243	0.09758	0.14636	0.19515
67	43	1.58451	2.37677	3.16903	0.09903	0.14855	0.19806
68	44	1.60782	2.41172	3.21563	0.10049	0.15073	0.20098
69	45	1.63112	2.44668	3.26224	0.10194	0.15292	0.20389
70	46	1.65442	2.48163	3.30884	0.1034	0.1551	0.2068
71	47	1.67772	2.51658	3.35544	0.10486	0.15729	0.20972
72	48	1.70102	2.55153	3.40205	0.10631	0.15947	0.21263
73	49	1.72432	2.58649	3.44865	0.10777	0.16166	0.21554
74	4A	1.74763	2.62144	3.49525	0.10923	0.16384	0.21845
75	4B	1.77093	2.65639	3.54186	0.11068	0.16602	0.22137
76	4C	1.79423	2.69135	3.58846	0.11214	0.16821	0.22428
77	4D	1.81753	2.7263	3.63506	0.1136	0.17039	0.22719
78	4E	1.84083	2.76125	3.68167	0.11505	0.17258	0.2301
79	4F	1.86414	2.7962	3.72827	0.11651	0.17476	0.23302
80	50	1.88744	2.83116	3.77487	0.11796	0.17695	0.23593
81	51	1.91074	2.86611	3.82148	0.11942	0.17913	0.23884
82	52	1.93404	2.90106	3.86808	0.12088	0.18132	0.24176
83	53	1.95734	2.93601	3.91468	0.12233	0.1835	0.24467
84	54	1.98064	2.97097	3.96129	0.12379	0.18569	0.24758
85	55	2.00395	3.00592	4.00789	0.12525	0.18787	0.25049

Table 13-5. Calculated Time-out Values (90-MHz Processor Clock) (Continued)

TMR[PS]		TMR[CLK] = 10 (System Bus Clock/16)			TMR[CLK] = 01 (System Bus Clock/1)		
Decimal	Hex	45 MHz	30 MHz	22.5 MHz	45 MHz	30 MHz	22.5 MHz
86	56	2.02725	3.04087	4.05449	0.1267	0.19005	0.25341
87	57	2.05055	3.07582	4.1011	0.12816	0.19224	0.25632
88	58	2.07385	3.11078	4.1477	0.12962	0.19442	0.25923
89	59	2.09715	3.14573	4.1943	0.13107	0.19661	0.26214
90	5A	2.12045	3.18068	4.24091	0.13253	0.19879	0.26506
91	5B	2.14376	3.21563	4.28751	0.13398	0.20098	0.26797
92	5C	2.16706	3.25059	4.33411	0.13544	0.20316	0.27088
93	5D	2.19036	3.28554	4.38072	0.1369	0.20535	0.27379
94	5E	2.21366	3.32049	4.42732	0.13835	0.20753	0.27671
95	5F	2.23696	3.35544	4.47392	0.13981	0.20972	0.27962
96	60	2.26026	3.3904	4.52053	0.14127	0.2119	0.28253
97	61	2.28357	3.42535	4.56713	0.14272	0.21408	0.28545
98	62	2.30687	3.4603	4.61373	0.14418	0.21627	0.28836
99	63	2.33017	3.49525	4.66034	0.14564	0.21845	0.29127
100	64	2.35347	3.53021	4.70694	0.14709	0.22064	0.29418
101	65	2.37677	3.56516	4.75354	0.14855	0.22282	0.2971
102	66	2.40007	3.60011	4.80015	0.15	0.22501	0.30001
103	67	2.42338	3.63506	4.84675	0.15146	0.22719	0.30292
104	68	2.44668	3.67002	4.89335	0.15292	0.22938	0.30583
105	69	2.46998	3.70497	4.93996	0.15437	0.23156	0.30875
106	6A	2.49328	3.73992	4.98656	0.15583	0.23375	0.31166
107	6B	2.51658	3.77487	5.03316	0.15729	0.23593	0.31457
108	6C	2.53988	3.80983	5.07977	0.15874	0.23811	0.31749
109	6D	2.56319	3.84478	5.12637	0.1602	0.2403	0.3204
110	6E	2.58649	3.87973	5.17297	0.16166	0.24248	0.32331
111	6F	2.60979	3.91468	5.21958	0.16311	0.24467	0.32622
112	70	2.63309	3.94964	5.26618	0.16457	0.24685	0.32914
113	71	2.65639	3.98459	5.31279	0.16602	0.24904	0.33205
114	72	2.67969	4.01954	5.35939	0.16748	0.25122	0.33496
115	73	2.703	4.05449	5.40599	0.16894	0.25341	0.33787
116	74	2.7263	4.08945	5.4526	0.17039	0.25559	0.34079
117	75	2.7496	4.1244	5.4992	0.17185	0.25777	0.3437
118	76	2.7729	4.15935	5.5458	0.17331	0.25996	0.34661
119	77	2.7962	4.1943	5.59241	0.17476	0.26214	0.34953
120	78	2.8195	4.22926	5.63901	0.17622	0.26433	0.35244
121	79	2.84281	4.26421	5.68561	0.17768	0.26651	0.35535
122	7A	2.86611	4.29916	5.73222	0.17913	0.2687	0.35826
123	7B	2.88941	4.33411	5.77882	0.18059	0.27088	0.36118
124	7C	2.91271	4.36907	5.82542	0.18204	0.27307	0.36409
125	7D	2.93601	4.40402	5.87203	0.1835	0.27525	0.367

Table 13-5. Calculated Time-out Values (90-MHz Processor Clock) (Continued)

TMR[PS]		TMR[CLK] = 10 (System Bus Clock/16)			TMR[CLK] = 01 (System Bus Clock/1)		
Decimal	Hex	45 MHz	30 MHz	22.5 MHz	45 MHz	30 MHz	22.5 MHz
126	7E	2.95931	4.43897	5.91863	0.18496	0.27744	0.36991
127	7F	2.98262	4.47392	5.96523	0.18641	0.27962	0.37283
128	80	3.00592	4.50888	6.01184	0.18787	0.2818	0.37574
129	81	3.02922	4.54383	6.05844	0.18933	0.28399	0.37865
130	82	3.05252	4.57878	6.10504	0.19078	0.28617	0.38157
131	83	3.07582	4.61373	6.15165	0.19224	0.28836	0.38448
132	84	3.09912	4.64869	6.19825	0.1937	0.29054	0.38739
133	85	3.12243	4.68364	6.24485	0.19515	0.29273	0.3903
134	86	3.14573	4.71859	6.29146	0.19661	0.29491	0.39322
135	87	3.16903	4.75354	6.33806	0.19806	0.2971	0.39613
136	88	3.19233	4.7885	6.38466	0.19952	0.29928	0.39904
137	89	3.21563	4.82345	6.43127	0.20098	0.30147	0.40195
138	8A	3.23893	4.8584	6.47787	0.20243	0.30365	0.40487
139	8B	3.26224	4.89335	6.52447	0.20389	0.30583	0.40778
140	8C	3.28554	4.92831	6.57108	0.20535	0.30802	0.41069
141	8D	3.30884	4.96326	6.61768	0.2068	0.3102	0.4136
142	8E	3.33214	4.99821	6.66428	0.20826	0.31239	0.41652
143	8F	3.35544	5.03316	6.71089	0.20972	0.31457	0.41943
144	90	3.37874	5.06812	6.75749	0.21117	0.31676	0.42234
145	91	3.40205	5.10307	6.80409	0.21263	0.31894	0.42526
146	92	3.42535	5.13802	6.8507	0.21408	0.32113	0.42817
147	93	3.44865	5.17297	6.8973	0.21554	0.32331	0.43108
148	94	3.47195	5.20793	6.9439	0.217	0.3255	0.43399
149	95	3.49525	5.24288	6.99051	0.21845	0.32768	0.43691
150	96	3.51856	5.27783	7.03711	0.21991	0.32986	0.43982
151	97	3.54186	5.31279	7.08371	0.22137	0.33205	0.44273
152	98	3.56516	5.34774	7.13032	0.22282	0.33423	0.44564
153	99	3.58846	5.38269	7.17692	0.22428	0.33642	0.44856
154	9A	3.61176	5.41764	7.22352	0.22574	0.3386	0.45147
155	9B	3.63506	5.4526	7.27013	0.22719	0.34079	0.45438
156	9C	3.65837	5.48755	7.31673	0.22865	0.34297	0.4573
157	9D	3.68167	5.5225	7.36333	0.2301	0.34516	0.46021
158	9E	3.70497	5.55745	7.40994	0.23156	0.34734	0.46312
159	9F	3.72827	5.59241	7.45654	0.23302	0.34953	0.46603
160	A0	3.75157	5.62736	7.50314	0.23447	0.35171	0.46895
161	A1	3.77487	5.66231	7.54975	0.23593	0.35389	0.47186
162	A2	3.79818	5.69726	7.59635	0.23739	0.35608	0.47477
163	A3	3.82148	5.73222	7.64295	0.23884	0.35826	0.47768
164	A4	3.84478	5.76717	7.68956	0.2403	0.36045	0.4806
165	A5	3.86808	5.80212	7.73616	0.24176	0.36263	0.48351

Table 13-5. Calculated Time-out Values (90-MHz Processor Clock) (Continued)

TMR[PS]		TMR[CLK] = 10 (System Bus Clock/16)			TMR[CLK] = 01 (System Bus Clock/1)		
Decimal	Hex	45 MHz	30 MHz	22.5 MHz	45 MHz	30 MHz	22.5 MHz
166	A6	3.89138	5.83707	7.78276	0.24321	0.36482	0.48642
167	A7	3.91468	5.87203	7.82937	0.24467	0.367	0.48934
168	A8	3.93799	5.90698	7.87597	0.24612	0.36919	0.49225
169	A9	3.96129	5.94193	7.92257	0.24758	0.37137	0.49516
170	AA	3.98459	5.97688	7.96918	0.24904	0.37356	0.49807
171	AB	4.00789	6.01184	8.01578	0.25049	0.37574	0.50099
172	AC	4.03119	6.04679	8.06238	0.25195	0.37792	0.5039
173	AD	4.05449	6.08174	8.10899	0.25341	0.38011	0.50681
174	AE	4.0778	6.11669	8.15559	0.25486	0.38229	0.50972
175	AF	4.1011	6.15165	8.20219	0.25632	0.38448	0.51264
176	B0	4.1244	6.1866	8.2488	0.25777	0.38666	0.51555
177	B1	4.1477	6.22155	8.2954	0.25923	0.38885	0.51846
178	B2	4.171	6.2565	8.342	0.26069	0.39103	0.52138
179	B3	4.1943	6.29146	8.38861	0.26214	0.39322	0.52429
180	B4	4.21761	6.32641	8.43521	0.2636	0.3954	0.5272
181	B5	4.24091	6.36136	8.48181	0.26506	0.39759	0.53011
182	B6	4.26421	6.39631	8.52842	0.26651	0.39977	0.53303
183	B7	4.28751	6.43127	8.57502	0.26797	0.40195	0.53594
184	B8	4.31081	6.46622	8.62162	0.26943	0.40414	0.53885
185	B9	4.33411	6.50117	8.66823	0.27088	0.40632	0.54176
186	BA	4.35742	6.53612	8.71483	0.27234	0.40851	0.54468
187	BB	4.38072	6.57108	8.76144	0.27379	0.41069	0.54759
188	BC	4.40402	6.60603	8.80804	0.27525	0.41288	0.5505
189	BD	4.42732	6.64098	8.85464	0.27671	0.41506	0.55342
190	BE	4.45062	6.67593	8.90125	0.27816	0.41725	0.55633
191	BF	4.47392	6.71089	8.94785	0.27962	0.41943	0.55924
192	C0	4.49723	6.74584	8.99445	0.28108	0.42161	0.56215
193	C1	4.52053	6.78079	9.04106	0.28253	0.4238	0.56507
194	C2	4.54383	6.81574	9.08766	0.28399	0.42598	0.56798
195	C3	4.56713	6.8507	9.13426	0.28545	0.42817	0.57089
196	C4	4.59043	6.88565	9.18087	0.2869	0.43035	0.5738
197	C5	4.61373	6.9206	9.22747	0.28836	0.43254	0.57672
198	C6	4.63704	6.95555	9.27407	0.28981	0.43472	0.57963
199	C7	4.66034	6.99051	9.32068	0.29127	0.43691	0.58254
200	C8	4.68364	7.02546	9.36728	0.29273	0.43909	0.58545
201	C9	4.70694	7.06041	9.41388	0.29418	0.44128	0.58837
202	CA	4.73024	7.09536	9.46049	0.29564	0.44346	0.59128
203	CB	4.75354	7.13032	9.50709	0.2971	0.44564	0.59419
204	CC	4.77685	7.16527	9.55369	0.29855	0.44783	0.59711
205	CD	4.80015	7.20022	9.6003	0.30001	0.45001	0.60002

Table 13-5. Calculated Time-out Values (90-MHz Processor Clock) (Continued)

TMR[PS]		TMR[CLK] = 10 (System Bus Clock/16)			TMR[CLK] = 01 (System Bus Clock/1)		
Decimal	Hex	45 MHz	30 MHz	22.5 MHz	45 MHz	30 MHz	22.5 MHz
206	CE	4.82345	7.23517	9.6469	0.30147	0.4522	0.60293
207	CF	4.84675	7.27013	9.6935	0.30292	0.45438	0.60584
208	D0	4.87005	7.30508	9.74011	0.30438	0.45657	0.60876
209	D1	4.89335	7.34003	9.78671	0.30583	0.45875	0.61167
210	D2	4.91666	7.37498	9.83331	0.30729	0.46094	0.61458
211	D3	4.93996	7.40994	9.87992	0.30875	0.46312	0.61749
212	D4	4.96326	7.44489	9.92652	0.3102	0.46531	0.62041
213	D5	4.98656	7.47984	9.97312	0.31166	0.46749	0.62332
214	D6	5.00986	7.51479	10.01973	0.31312	0.46967	0.62623
215	D7	5.03316	7.54975	10.06633	0.31457	0.47186	0.62915
216	D8	5.05647	7.5847	10.11293	0.31603	0.47404	0.63206
217	D9	5.07977	7.61965	10.15954	0.31749	0.47623	0.63497
218	DA	5.10307	7.6546	10.20614	0.31894	0.47841	0.63788
219	DB	5.12637	7.68956	10.25274	0.3204	0.4806	0.6408
220	DC	5.14967	7.72451	10.29935	0.32185	0.48278	0.64371
221	DD	5.17297	7.75946	10.34595	0.32331	0.48497	0.64662
222	DE	5.19628	7.79441	10.39255	0.32477	0.48715	0.64953
223	DF	5.21958	7.82937	10.43916	0.32622	0.48934	0.65245
224	E0	5.24288	7.86432	10.48576	0.32768	0.49152	0.65536
225	E1	5.26618	7.89927	10.53236	0.32914	0.4937	0.65827
226	E2	5.28948	7.93423	10.57897	0.33059	0.49589	0.66119
227	E3	5.31279	7.96918	10.62557	0.33205	0.49807	0.6641
228	E4	5.33609	8.00413	10.67217	0.33351	0.50026	0.66701
229	E5	5.35939	8.03908	10.71878	0.33496	0.50244	0.66992
230	E6	5.38269	8.07404	10.76538	0.33642	0.50463	0.67284
231	E7	5.40599	8.10899	10.81198	0.33787	0.50681	0.67575
232	E8	5.42929	8.14394	10.85859	0.33933	0.509	0.67866
233	E9	5.4526	8.17889	10.90519	0.34079	0.51118	0.68157
234	EA	5.4759	8.21385	10.95179	0.34224	0.51337	0.68449
235	EB	5.4992	8.2488	10.9984	0.3437	0.51555	0.6874
236	EC	5.5225	8.28375	11.045	0.34516	0.51773	0.69031
237	ED	5.5458	8.3187	11.0916	0.34661	0.51992	0.69323
238	EE	5.5691	8.35366	11.13821	0.34807	0.5221	0.69614
239	EF	5.59241	8.38861	11.18481	0.34953	0.52429	0.69905
240	F0	5.61571	8.42356	11.23141	0.35098	0.52647	0.70196
241	F1	5.63901	8.45851	11.27802	0.35244	0.52866	0.70488
242	F2	5.66231	8.49347	11.32462	0.35389	0.53084	0.70779
243	F3	5.68561	8.52842	11.37122	0.35535	0.53303	0.7107
244	F4	5.70891	8.56337	11.41783	0.35681	0.53521	0.71361
245	F5	5.73222	8.59832	11.46443	0.35826	0.5374	0.71653

Table 13-5. Calculated Time-out Values (90-MHz Processor Clock) (Continued)

TMR[PS]		TMR[CLK] = 10 (System Bus Clock/16)			TMR[CLK] = 01 (System Bus Clock/1)		
Decimal	Hex	45 MHz	30 MHz	22.5 MHz	45 MHz	30 MHz	22.5 MHz
246	F6	5.75552	8.63328	11.51103	0.35972	0.53958	0.71944
247	F7	5.77882	8.66823	11.55764	0.36118	0.54176	0.72235
248	F8	5.80212	8.70318	11.60424	0.36263	0.54395	0.72527
249	F9	5.82542	8.73813	11.65084	0.36409	0.54613	0.72818
250	FA	5.84872	8.77309	11.69745	0.36555	0.54832	0.73109
251	FB	5.87203	8.80804	11.74405	0.367	0.5505	0.734
252	FC	5.89533	8.84299	11.79065	0.36846	0.55269	0.73692
253	FD	5.91863	8.87794	11.83726	0.36991	0.55487	0.73983
254	FE	5.94193	8.9129	11.88386	0.37137	0.55706	0.74274
255	FF	5.96523	8.94785	11.93046	0.37283	0.55924	0.74565